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Ranage Gate Generator Development for 10kHz Laser Ranging

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Abstract. *Korea Astronomy and Space Science institute (KASI) is developing the new range gate generator, called A-RGG, for 10kHz laser ranging. The A-RGG is designed based on GRAZ ISA Card but range gate (RG) is computed in FPGA H/W of A-RGG using Lagrange interpolation instead of PC program. The A-RGG consists of RG signal generator for C-SPAD, FIRE signal generator, 3 OUTPUT ports to control external device and LED indicator. The RG signal generator calculates the expected laser arrival time returned from satellites by using lookup table transferred from the operation system. It can also support the calibration ranging even though the ground target has short distance. The FIRE signal generator controls the laser system to fire a laser pulse and conducts laser collision avoidance against backscattering. The period and pulse width of FIRE signal is controlled by external program. The pulse start time and width of signals in 3 OUTPUT ports are also programmable, which can be synchronized with RG or FIRE signal. The LED indicator shows internal operation status. All functions of A-RGG are controlled through serial communication.*

1. Features

Lagrange interpolation method : FPGA (Stratix 2P2S30S)
Lagrange calculation time : 65.65μs(@50MHz)
Lookup table Memory : 256 x 64bit x 2
FIFO memory : 32,768 x 48bit
Delay generation : Digital delay(DS1023S-50)
Operation mode : Range, Ground calibration, Overlap avoidance, Dual selection satellite(A,B)
Operation control : Serial or TCP/IP
Resolution : RGG generator - 0.5ns, Internal Event timer - 0.5ns, FIRE signal - 100ns
Timing input signal : 1PPS, 10MHz, IRG-B
Input signal : START, IN1
Output signal : RGG, FIRE, Out1~3(Sync with RGG or FIRE, variable width)
LED indicator for I/O port : 1PPS, 10MHz, IRIG-B, START, IN1, RGG, FIRE, Out1~3
Status FND Display :

- UTC(Day, Hour, Min, Second)
- Range(ns)
- Laser Fire(Set, measure)
- FIFO(Number of Fires in the sky)

Figure 1. Front panel of A-RGG

2. A-RGG Functional Block

The A-RGG consists of communication, display, timing, Lagrange processor and SLR application block to generate RGG and FIRE signal. The communication block receives configuration command and lookup data from PC by serial or TCP/IP. The Timing Block generates internal timing signal of A-RGG using 10MHz, 1PPS, IRIG-B from GPS Timing reference. The Lagrange processor interpolates TOF using Lagrange method by 64bit or 128bit fast arithmetic logic unit. The SLR application block generate FIRE and RGG signal using configuration data form PC and calculated result of Lagrange processor. The FIRE signal is generated based on the frequency set by PC, but its generation pauses when it overlap to the returned signal from satellite. The display controller displays internal operation status of A-RGG to LED and FND

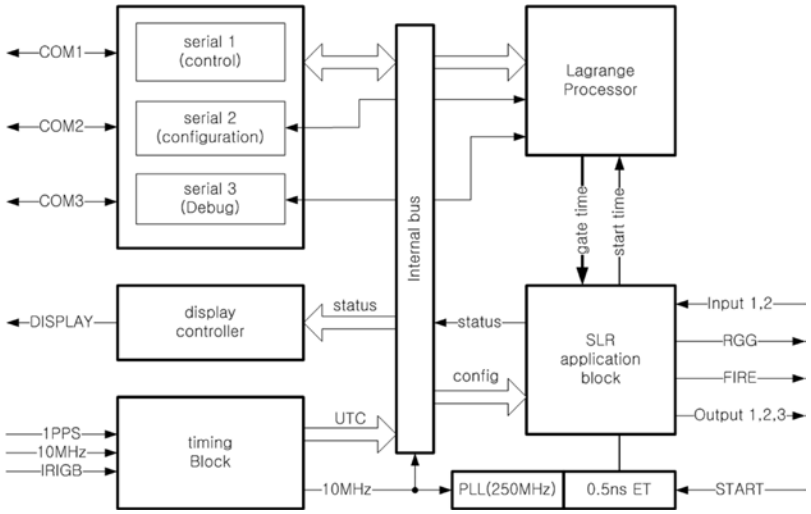

Figure 2. Top level functional block diagram of A-RGG

3. Sync signal & OUTPUT Port

The A-RGG have 5 OUTPUT ports; FIRE, OUT1~3 and RGG. The OUTPUT circuit uses 10MHz as the reference frequency. The 10MHz signal is delivered through separate signal line to each block in order to compensate fan out. The 1PPS_10M_sync line is a 10MHz signal synchronized with 1PPS which delivers through one line to each block to match sync between each block. The FIRE and OUTPUT 1~3 have 100ns period, which also use 10MHz signal for reference. The resolution of RGG is 0.5ns using external digital delay chip which use 10MHz reference signal.

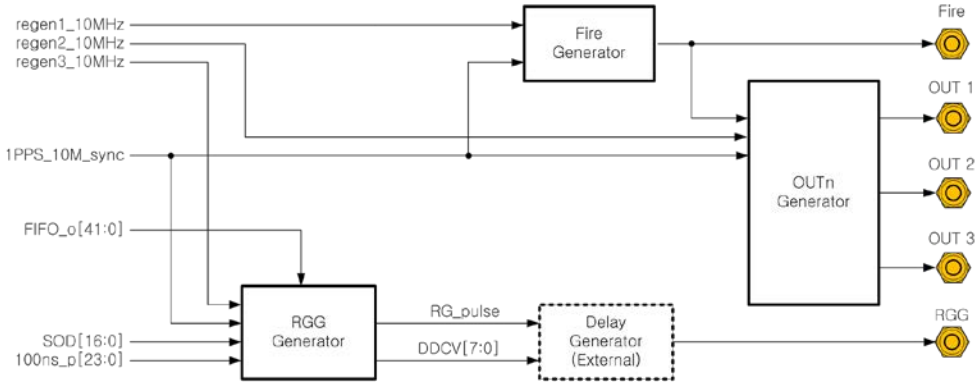

Figure 3. The block diagram of Range Gate Generation & Output

4. Timing Block

The ARGG sampling clock of laser START signal is 200MHz which is generated by PLL. The reference clock of the PLL is 10MHz from GPS Timing reference. The resolution of START signal is 0.5ns based on 5ns(200MHz) resolution using FPGA logic delay chain. The RGG epoch time is combination of measured START epoch time and IRIG-B time information.

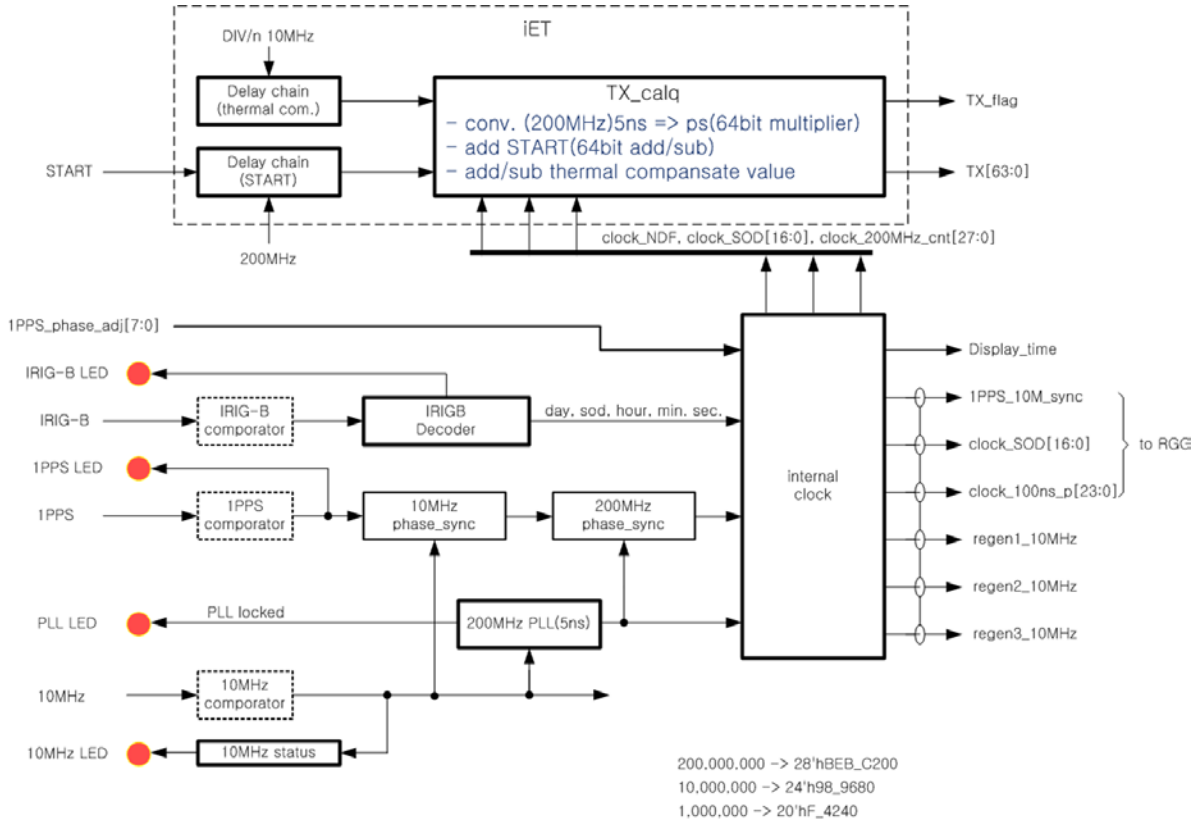

Figure 4. Internal clock generation block of A-RGG

The AM-modulated IRIG-B signal detection uses a simple H/W comparator. UTC time is restored by sync decoder, bit decoder and byte decoder after sampling part of “1” in entered IRIG-B signal.

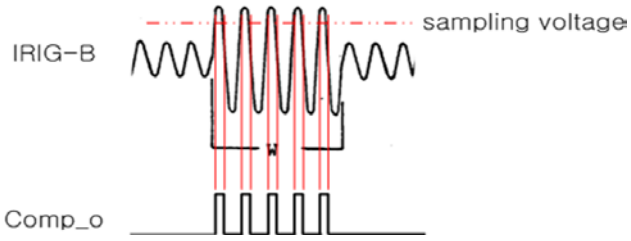

Figure 5. Modulated carrier of IRIG-B signal & sampling voltage

5. Lagrange processor

The Lagrange processor in the A-RGG dedicates to Lagrange interpolation which consists of basic arithmetic logic unit(64bit adder/ subtractor, multiplier, divider etc..). The arithmetic logic unit usually operates 64bit. To improve accuracy of calculation, a 128-bit divider is also used. The Lagrange calculation is performed by fixed method and applys 2’s complement scalier for

significantly fast calculation speed. This calculation uses micro code method which performs calculation by fixed sequence when START time value is delivered. Micro code method increases circuit usage efficiency by reusing high speed ALU. As a result of using micro code method, size of circuit is decreased. The calculation time of Lagrange interpolation is 65 μs and fire rate can be 15 KHz.

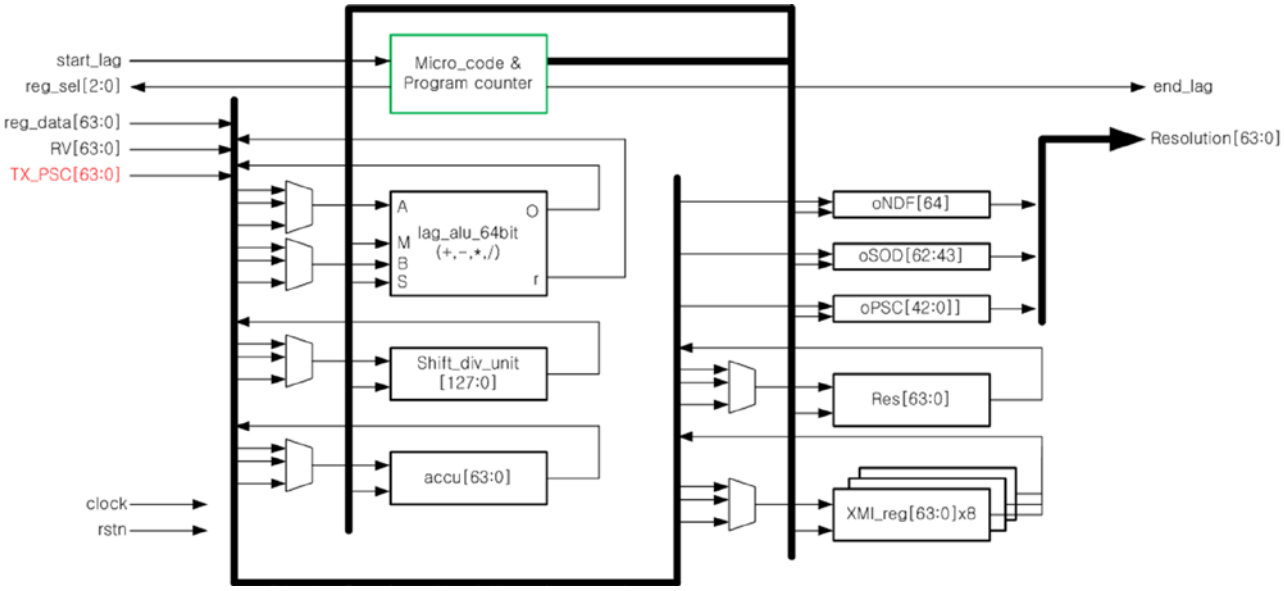

Figure 6. 64-bit Lagrange processor

6. Functional verification S/W

The functional verification S/W of the A-RGG is performed using Matlab. This S/W consists of two programs to verify function and performance of the A-RGG respectively. Data communication between PC and A-RGG uses serial communication. Register and memory are configured by functional verification program. Register is configured to control each part of A-RGG. For increasing reliability of equipment, this program has also simulation feature to check A-RGG lagrange calculation in PC. The performance verification program can read .pdt file and downloads to A-RGG for real-time experiments. Experiments for various satellites can be easily performed by using this program. Data and results used in experiments can be checked by graph.

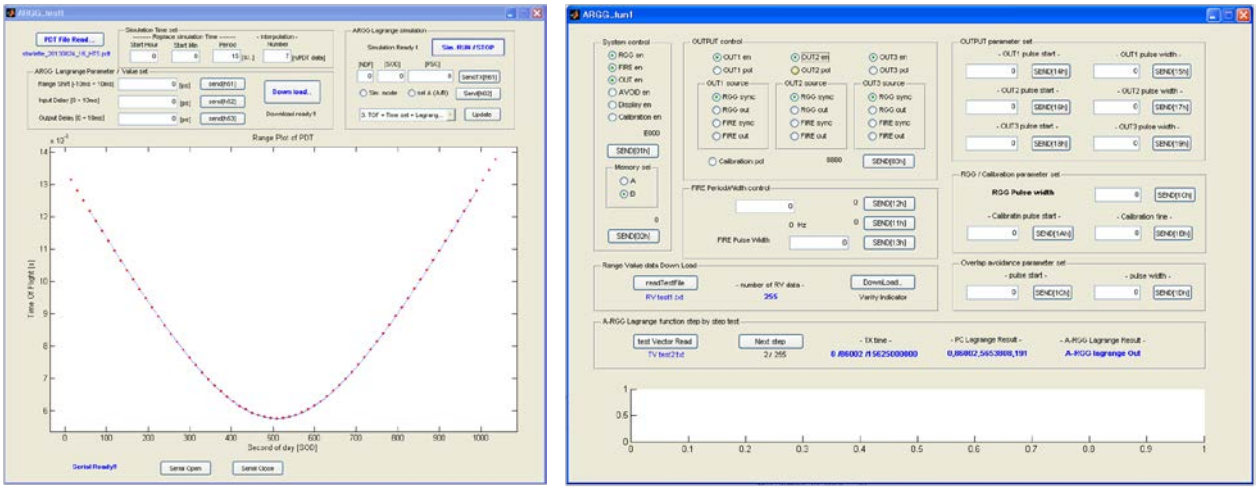

Figure 7. The functional verification S/W of the A-RGG