New KHz capable software in Metsähovi

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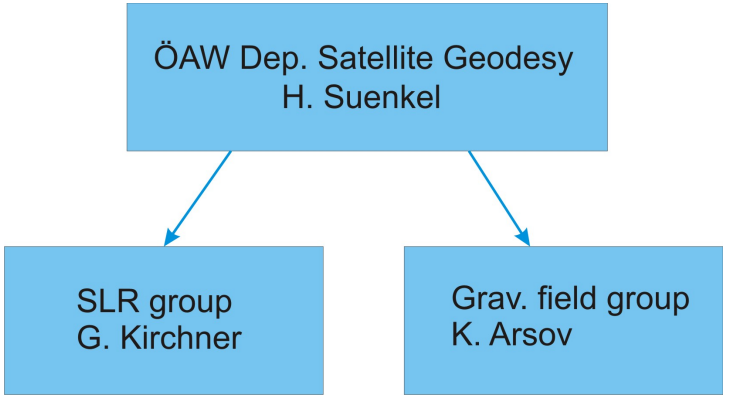
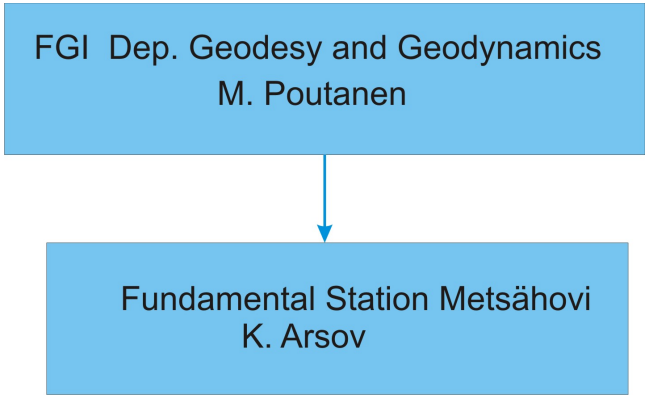
Short Bio

Before Finland



Currently



Short Bio

Before Finland

Currently

2007-cur Responsiblle for Metsähovi Fundamental station in general and SLR in particular. Work concentrated on the new 2KHz SLR in Metsähovi; inplementation of all the new hardware+software and fine tunning the system. Research also on Satellite Geodesy in general and Gravity from space in particular.

Some Department Tasks

- EUREF and its realisation in Finland (EUREF-FIN), connection to the international frames
- Vertical datums, precise levelling, and new Finnish height system, participation in the creation of new European vertical datum
- Participation on IAG services (IGS, IVS, ILRS, IDS) and other international permanent geodetic networks (EPN, GGP, NGOS, GGOS ...), especially using FinnRef and the instrumentation in Metsähovi
- Promotion, education and consultation on new reference frames in Finland;

Metsähovi Observatory

- Research unit of FGI, Department of Geodesy and Geodynamics

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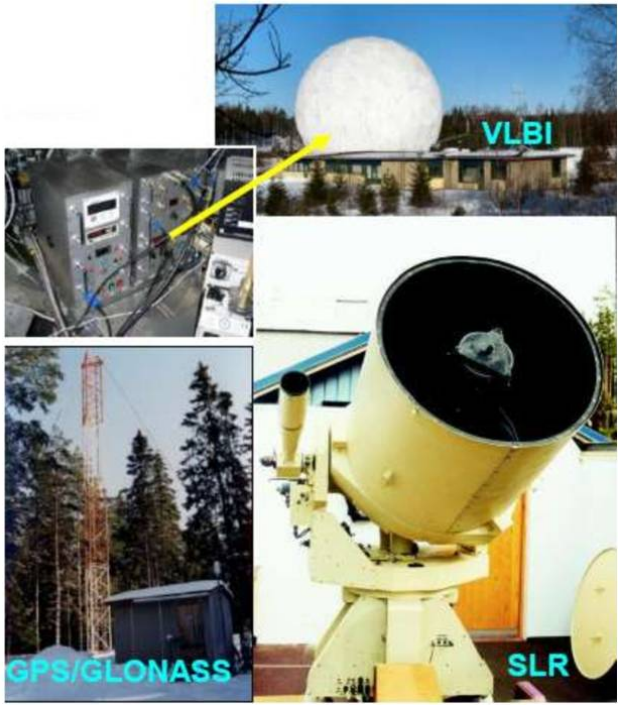
Metsähovi Instrumentation

- GPS (IGS station since 1992)



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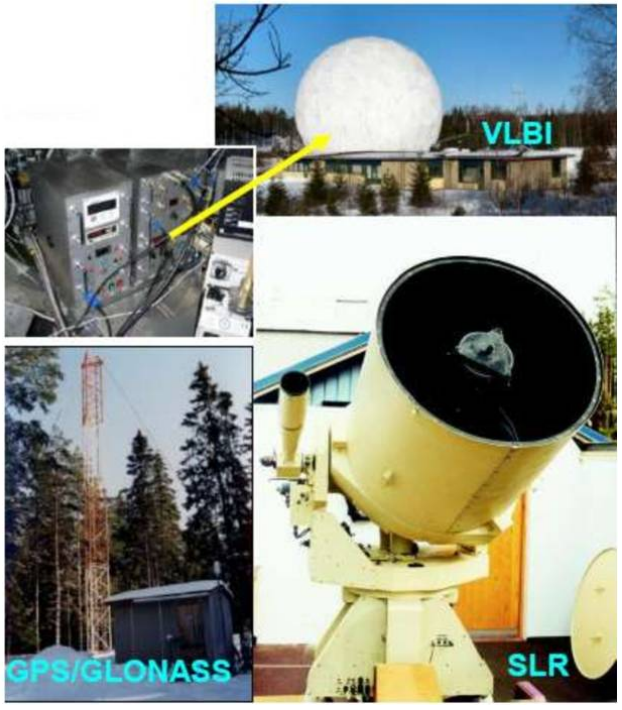

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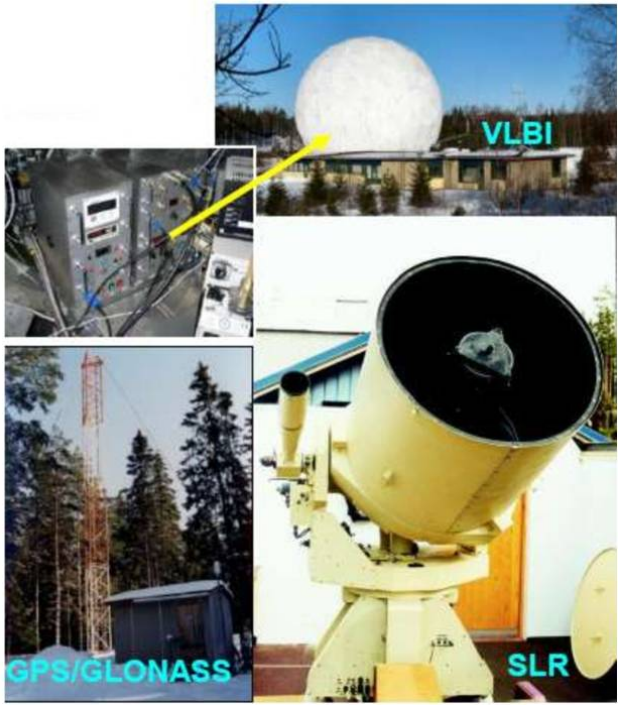

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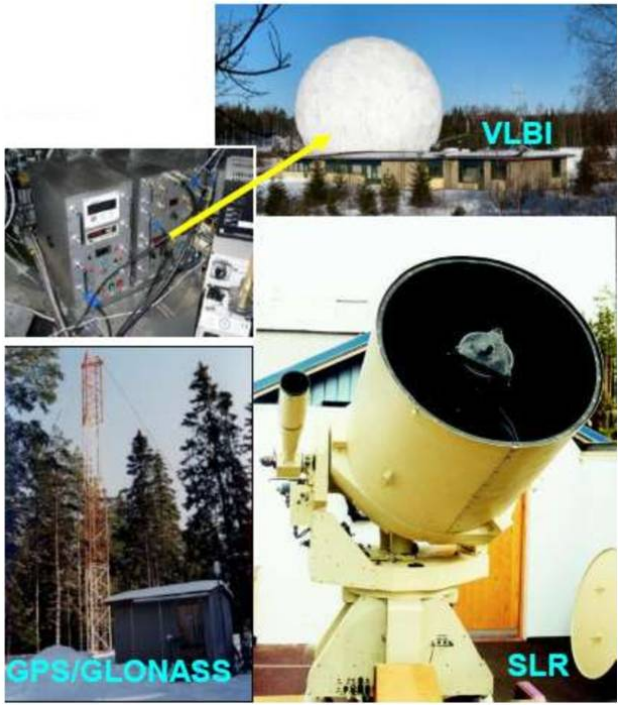
- geo-VLBI (2004- curr)



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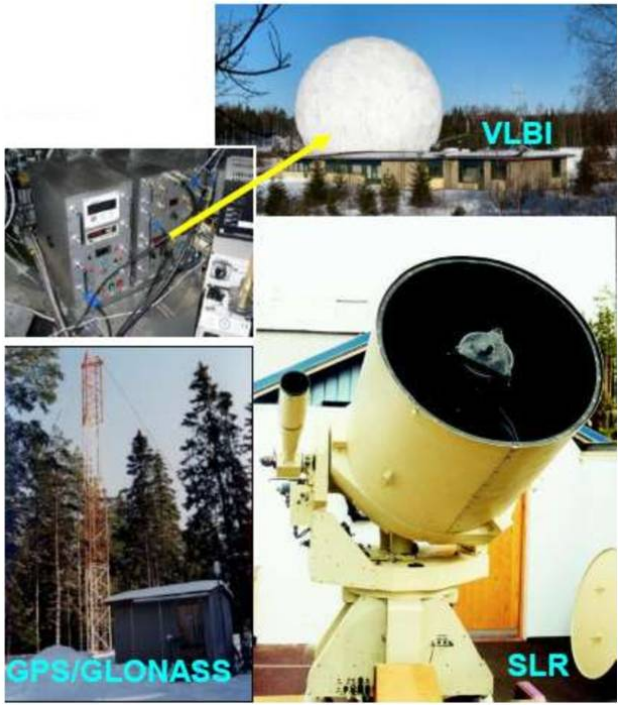

Metsähovi Instrumentation

- GPS (IGS station since 1992)
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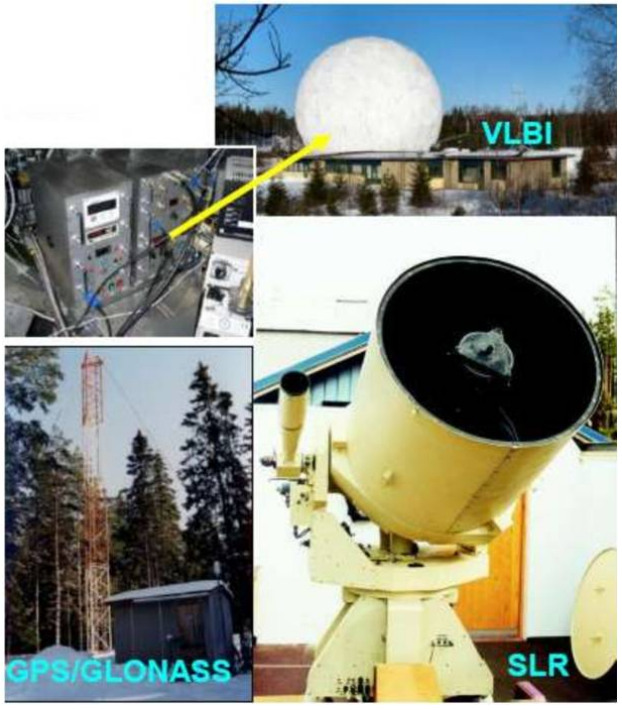
- geo-VLBI (2004- curr)
- DORIS
- SCG



Metsähovi Instrumentation

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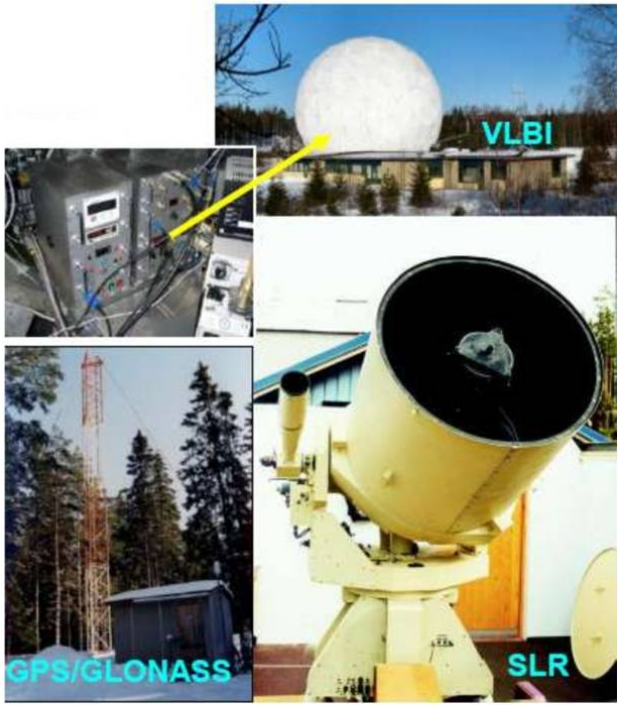
- DORIS
- SCG
- Abs. Gravity



Metsähovi Instrumentation

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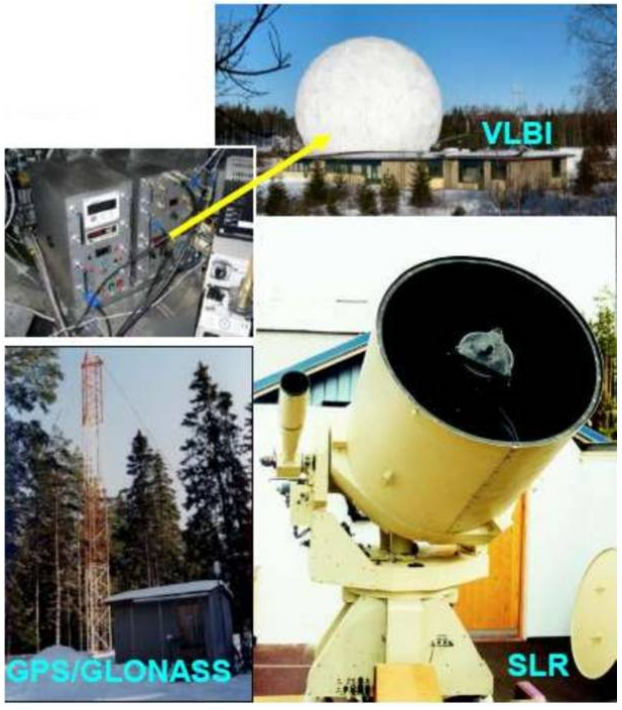
- DORIS
- SCG
- Abs. Gravity
- Seismometer



SLR general

- Not operational from second half of 2005
- Old 1Hz system; difficult maintenance and observations, most of equipment old and obsolete.
- Personnel change; late 2006 decision to completely renovate the system; started Apr 2007.
- New laser late 2006, HighQ 2KHz, Nd:VAN solid state laser., pulse 12.3ps 830mW, 0.425mJ @532nm.
- Purchase of A032-ET for 2KHz timing
- Graz+own fpga based RGG board for time critical tasks.
- UTC timing; GPS time + frequency receiver from CNSSYS (used frequently in VLBI);Serves also as NTP time server.
- Meteo server; Vaisala PTU200 (in the station at the moment 5 barometers present)

SLR general

- New photodetector C-SPAD replaced the old PMT.
- Couple of pulse distributors.
- Timing signal from H. Maser.
- New encoders for the telescope together with motors, complete renovation of the telescope is undergoing.
- New room for SLR instrumentation.
- New operational software from scratch to suit the new 2KHz SLR.
- Primary telescope mirror recoated.
- Mechanical/optical solution for the separate beam path under implementation.
- Seeking funding for a new telescope and a dome to host the new SLR observatory building in the future

SLR software outlilne

2KHz software

- Windows 7 operating system with intel i9 -> 8 threads.
- Operator knowledge only how to use mouse.
- RTOS not needed because of:
  - Windows is never later then 1 msec. Especially in loops, threads or services.
  - Running only the most necessary services.
  - All time critical tasks are programmed as windows services or threads or executed in hardware.
  - A032-ET has FIFO buffers, so no need for real-time.
  - All fpga board tasks done in FIFOs.
  - Min "idle" requirement is ToF. GOCE 1.5-2 ms.
  - Graphics is done with DirectX10 inside graphics board. Partly is programmed as video game.
  - Full GUI implementation with MFC library.

SLR software outlilne

2KHz software

- RTOS not needed because of: (cnt.)
  - all writings to disk are done binary in threads writing big amount of data at once; ex. write everything after 5 min observing from service.
  - all interpolations, computations etc from threads.
- Writing everything new from scratch tailored to 2KHz system
  - C++ as programming language +MFC and partly Assembler.
- RGG -> fpga, hardware accelerated, couple of event timers inside, laser control, C-SPAD etc.
- Master windows computer for session planning, SLR measurement, Graphics, 1Gb LAN for time telescope and meteo server communication.
- design of our own fpga SLR controller board based on Graz DOS ISA board.

SLR software outlilne

2KHz software

- PCI and win instead of ISA and DOS
- 150 €board with our own software
- Automatic session downloading, CPF treatment, session planning, observation etc.
- Graphics rendering, computations, display controlled by the graphics external board, no additional burden on CPU.
- Full 2KHz scenario uses only 20% of the CPU.
- Capable of 10KHz observations scenario.
- Use of LAVA PCIe for timer reading.
- User/administrator usage for preserving modifying the properties/sessions.
- 1s screenshots copied to ftp server for documentation.

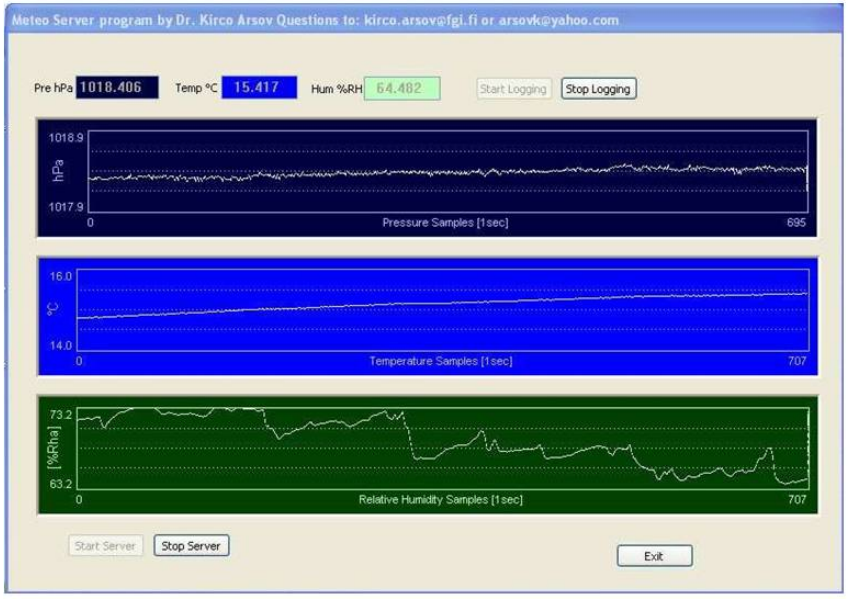
And very important...

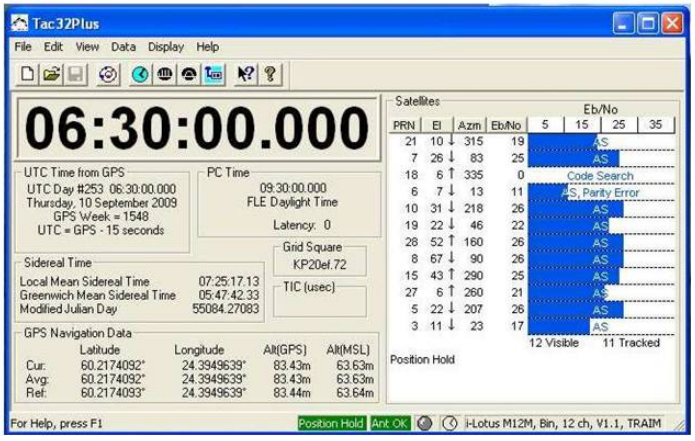
IT IS FREE TO ANYONE INTERESTED!!

(GPL) licence; Code freely available to SLR community!

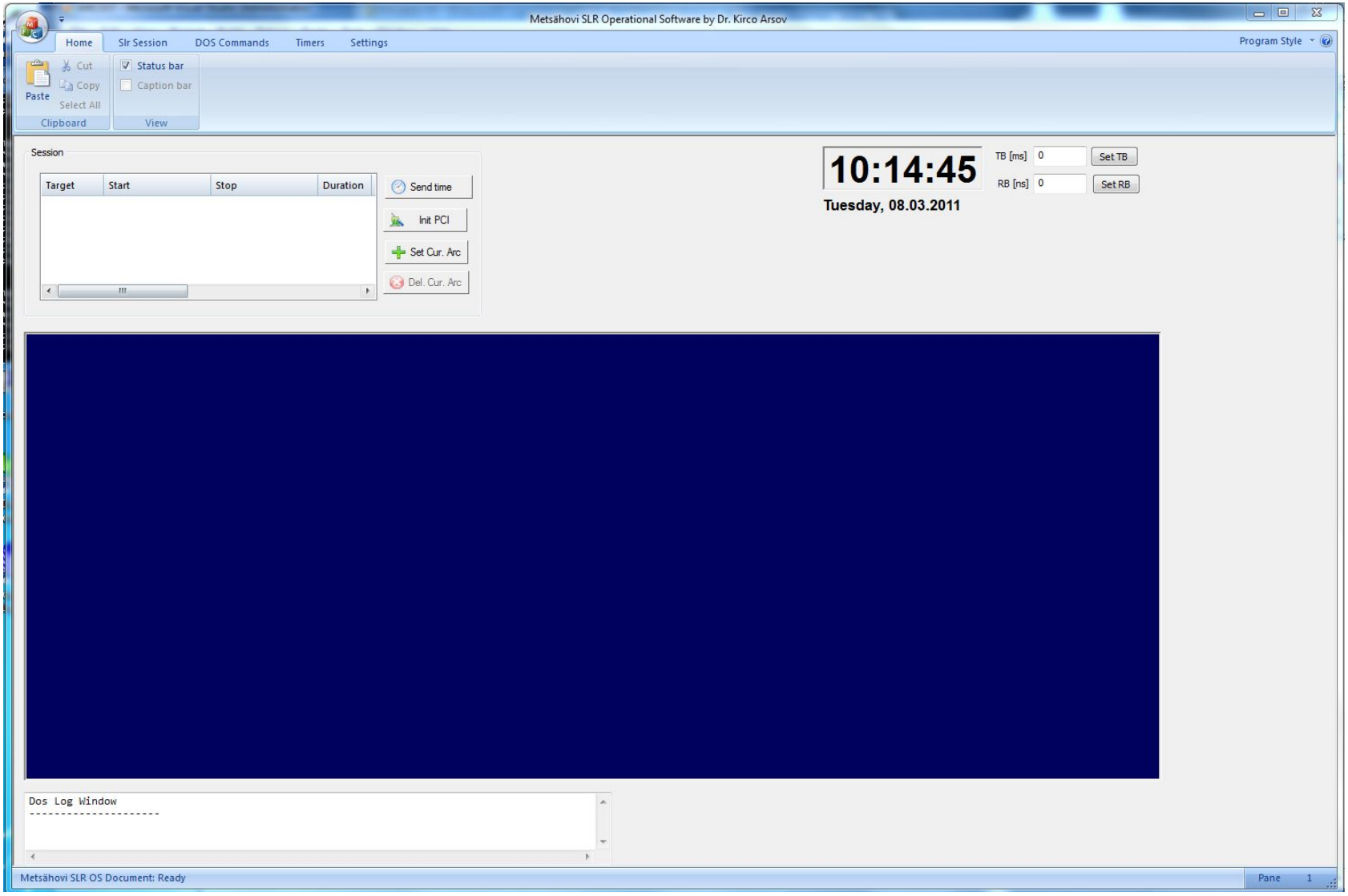
SLR meteo + UTC

- Own program for Meteo data and NTP
- CNSClock II for UTC offset

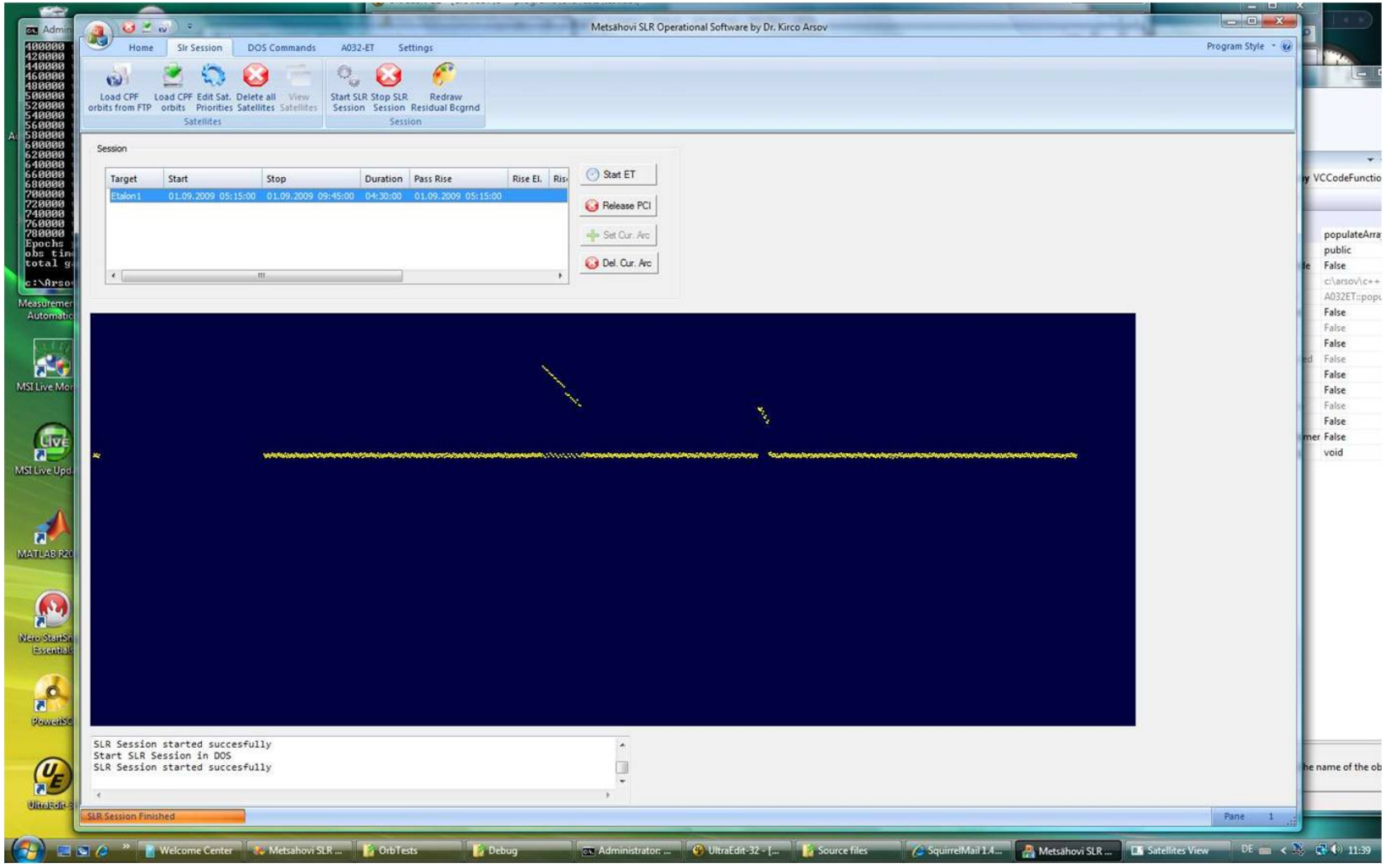




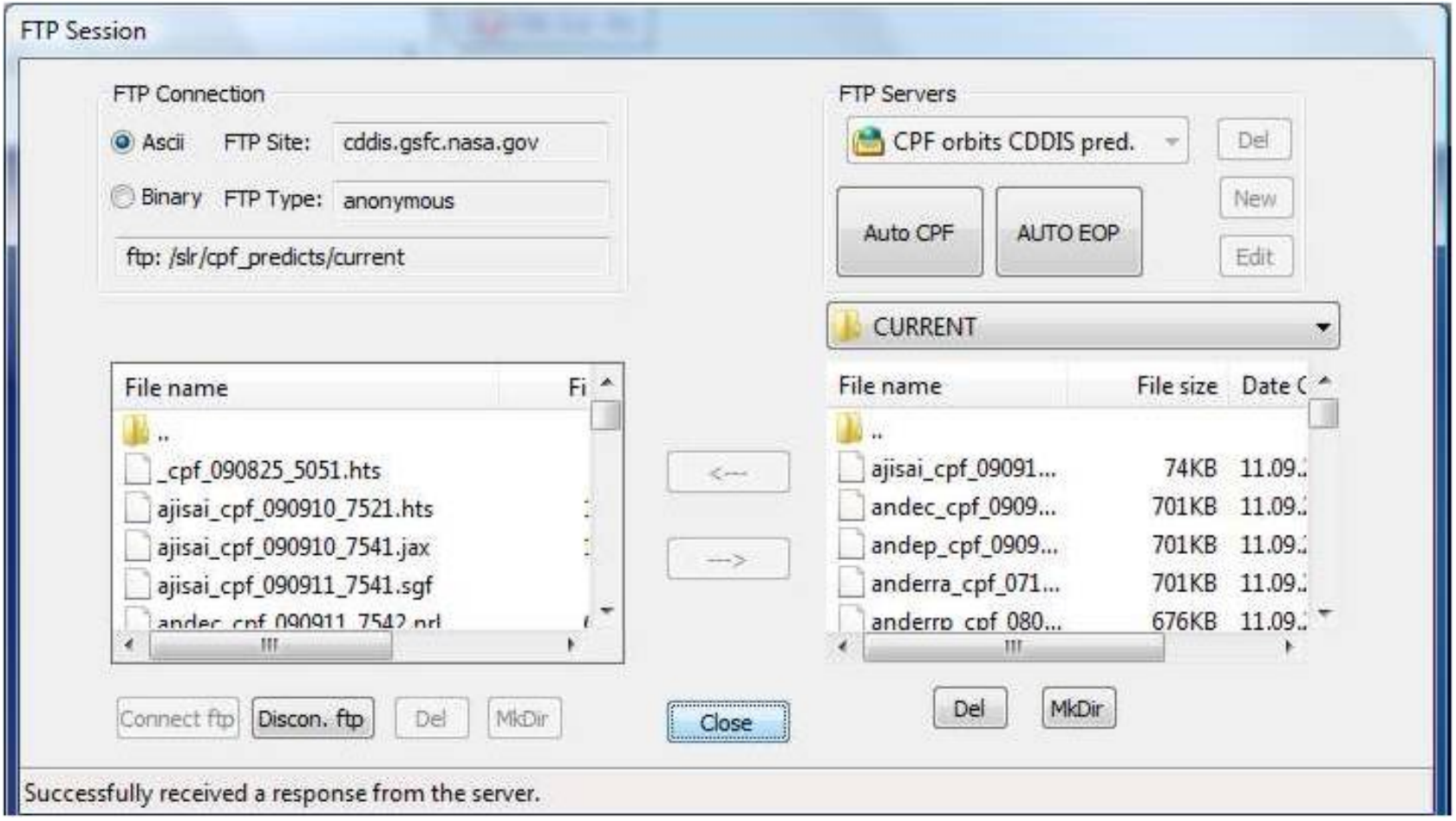
SLR software



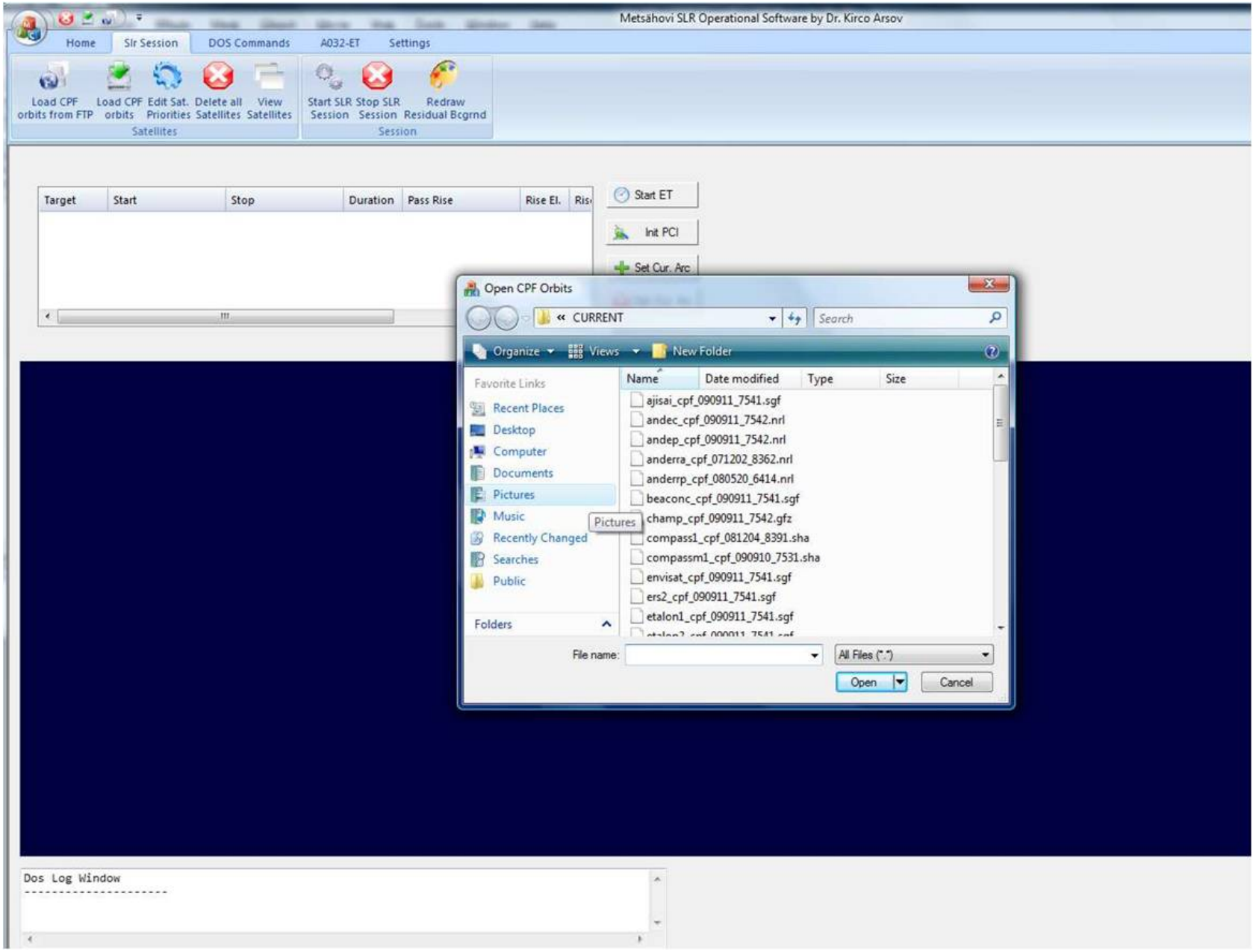
SLR A032-ET overlapping



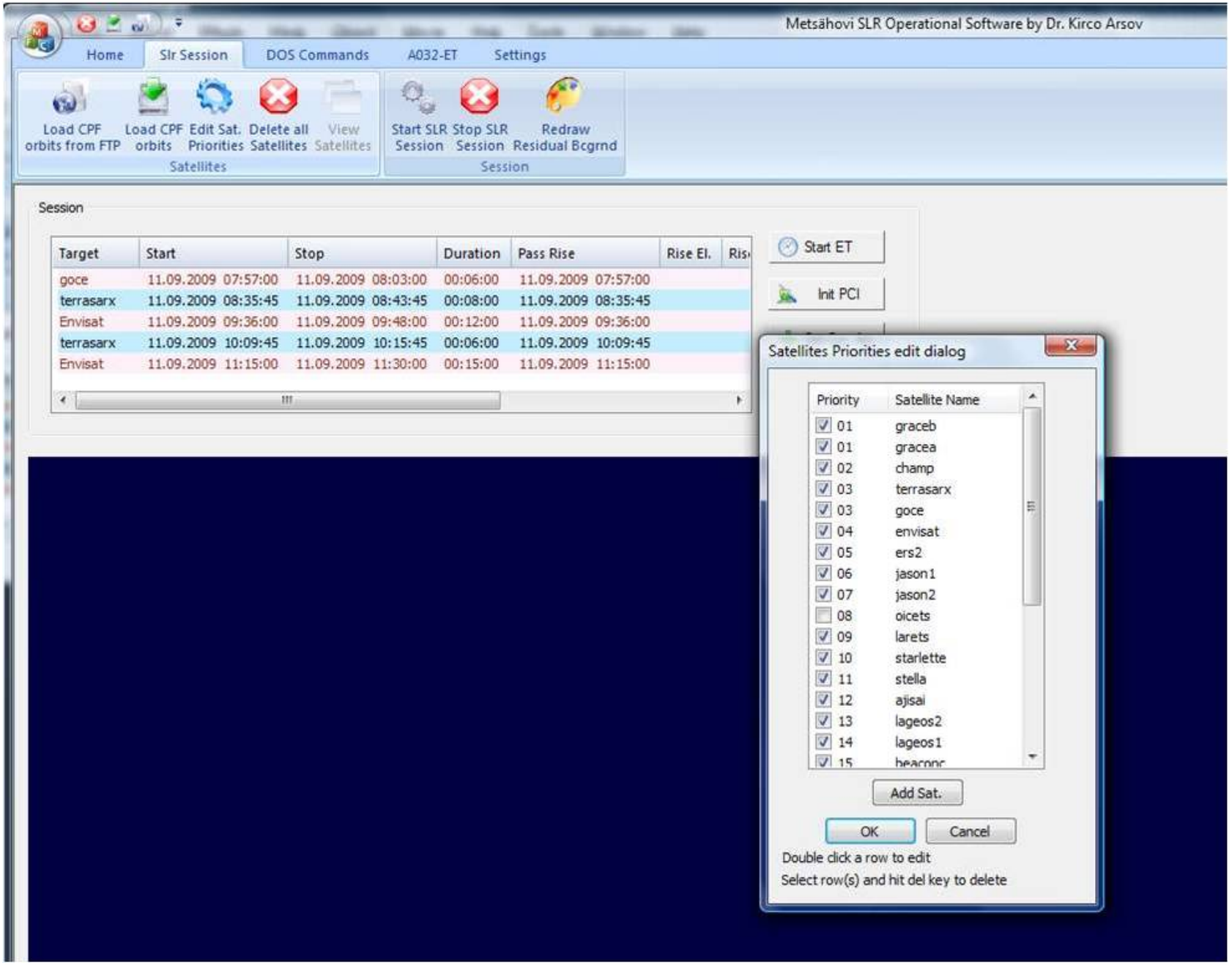
SLR ftp cpf orbits



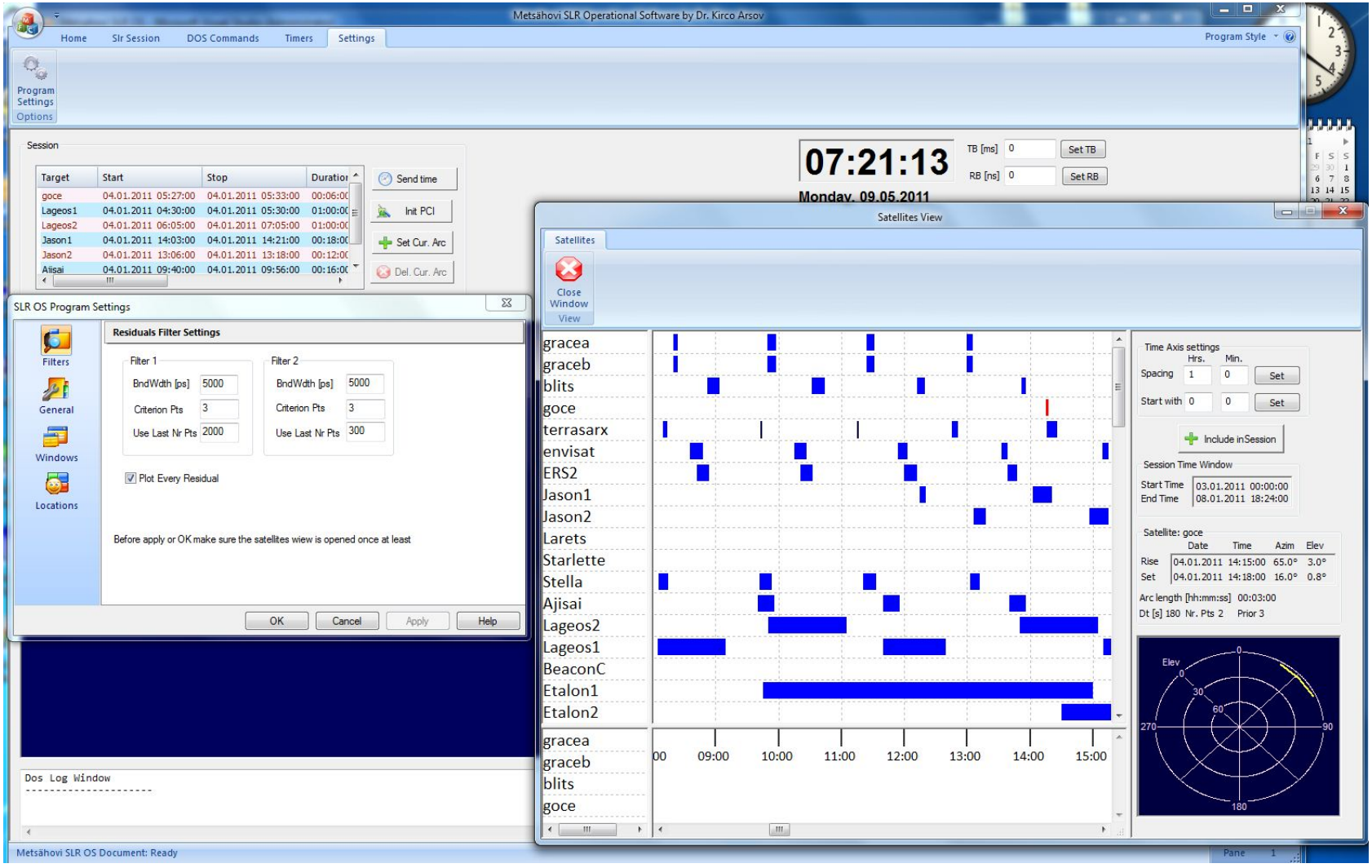
SLR load cpf orbits



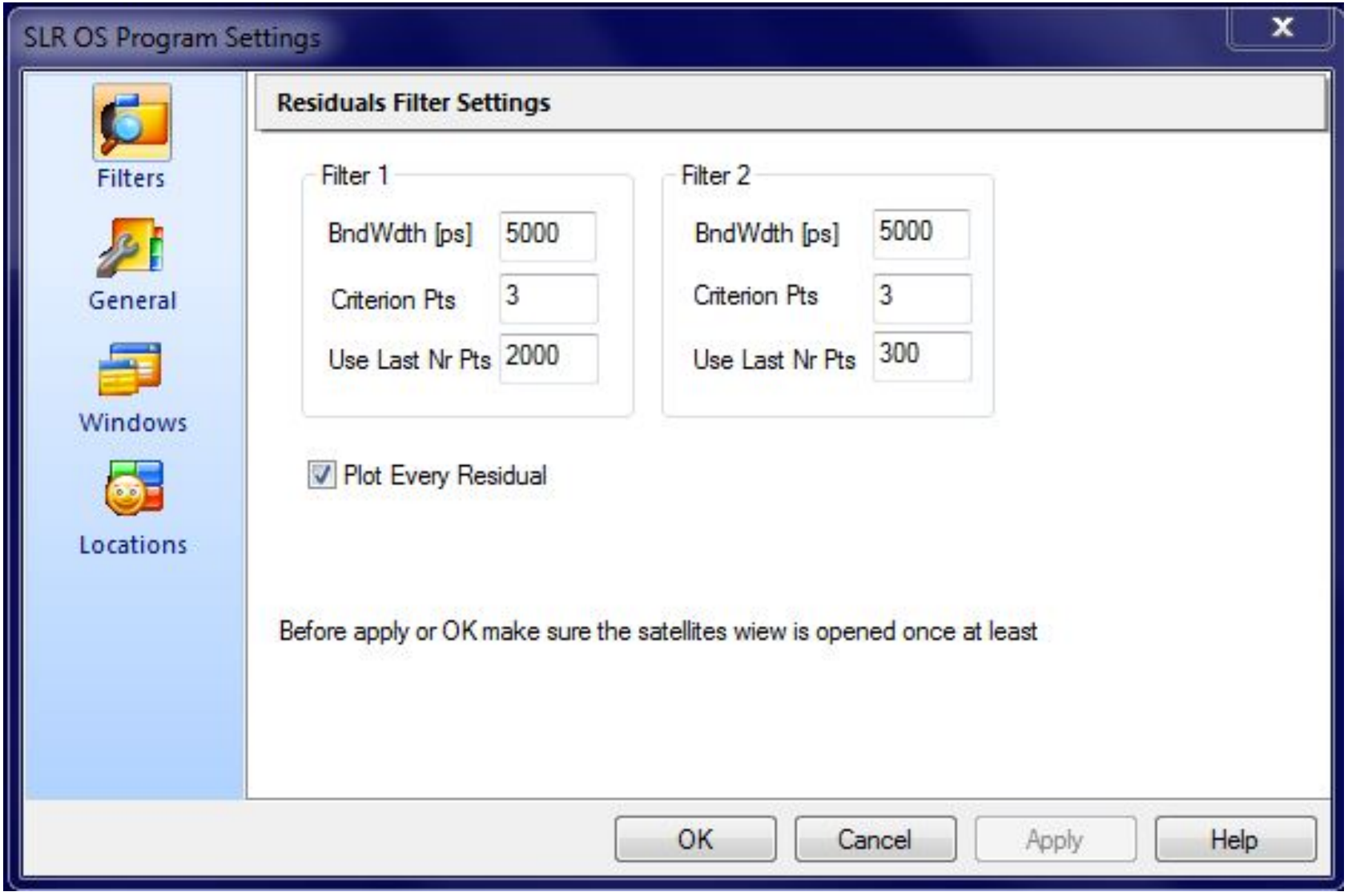
SLR satellites management



SLR residuals filter



SLR residuals filter



SLR software future work

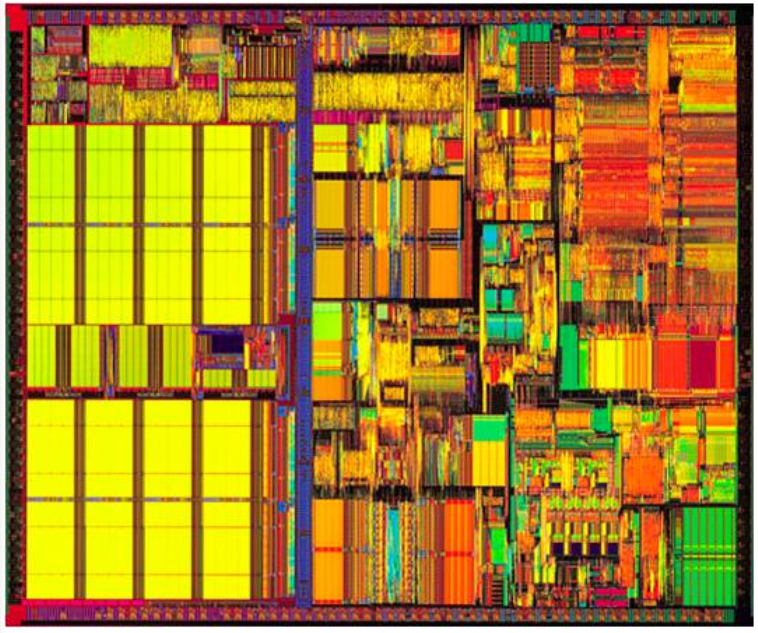
to do...

- PCIe FPGA implementation
- Smart satellite search, auto RB, TB determination and setting in real time
- Auto RG_WIDTH setting
- Kalman to aid in filtering ?
- Auto session planning, real time visibility and sat plot
- Post processing module (use Graz/RIGA version for starting)
- Telescope control module
- Work on higher rates ?
- More automation
- Virtual observation animation

FPGA SLR developments; CPU vs FPGA

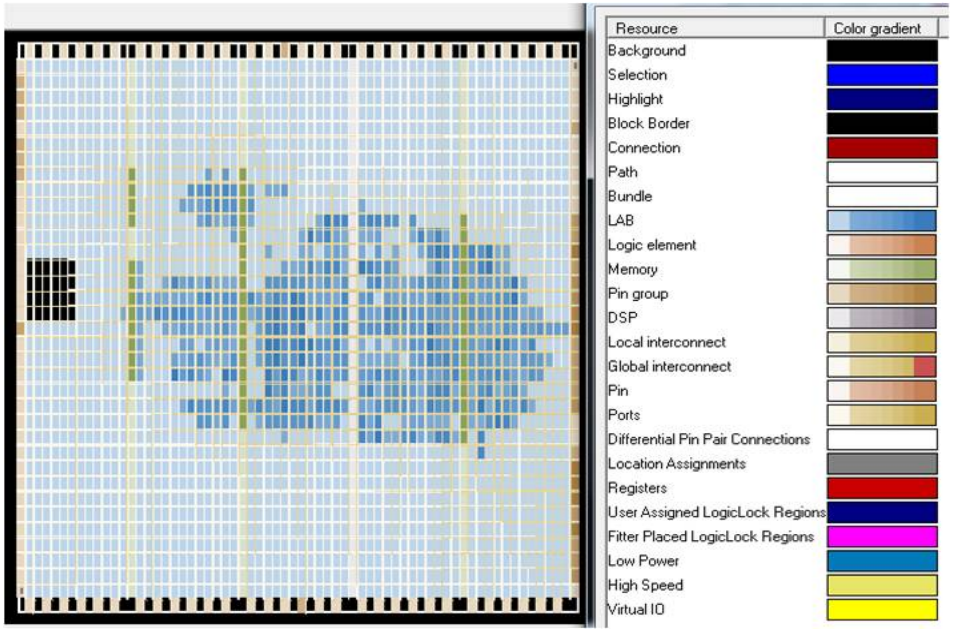
- **Field Programmable Gate Array (FPGA)**: Executes all "instructions" in parallel.
- You write massively parallel source code for FPGA. Code is translated directly into hardware.
- You can even fit small computers on a single FPGA (Commodore-64 is popular). FPGA chips have hundreds of free I/O pins you can use for whatever you like: DDR2 busses, PCI busses, motor and robot control, switch-mode supplies, timing systems, ... SLR telescope control?

FPGA vs CPU

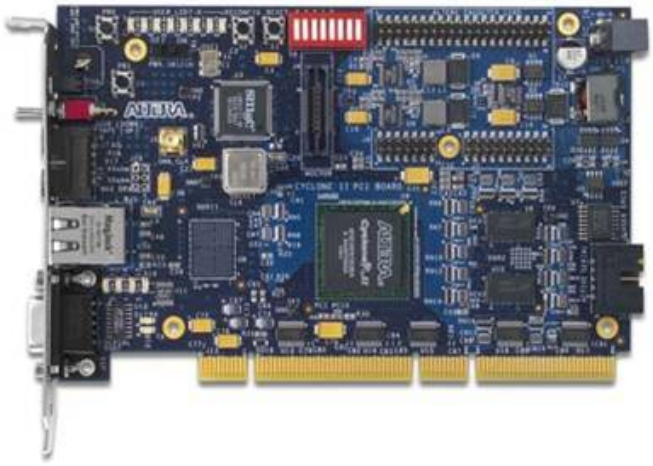


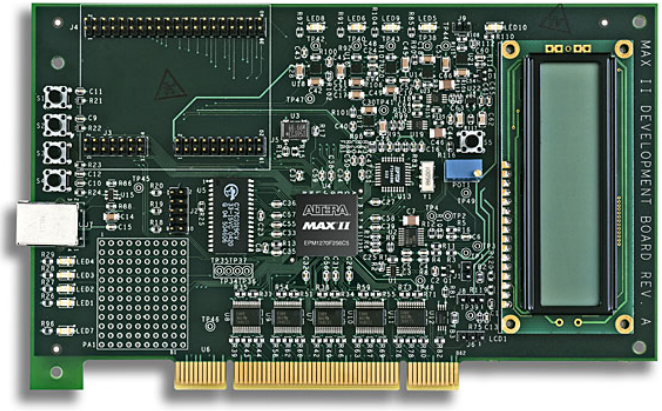
- **SLR code translated onto FPGA (500++tasks/cycle?)**
  Green=memory, blue=SLR logic, light blue=free

- **Intel Celeron CPU (1 task/Cycle)**



FPGA project; Hardware used





PCI and PCI-X	PCIe 1.x/2.0/3.0
Obsolete	The standard
Already faster than SLR requires	Even faster, ≥250MB/s/lane
Cheap sub-$1k evaluation kits	Kits reasonably inexpensive
Easy to design 66MHz boards	Challenging to make GHz boards
Free PCI software cores for FPGA	Only commercial cores costing ≥$5000/license

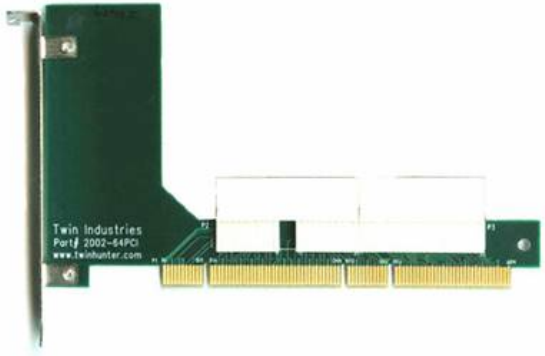
Altera PCI/PCI-X Evaluation Kit €800 Based on a small CycloneII FPGA (EP2C35). MAXII CPLD development kit, €150 -> Open code to SLR community

Next...

Future: Altera CycloneIII or Xilinx Spartan3 micromodules
=€100, same SLR functionality!

OR

+



Just add water (or PCI card edge ☺)

Current status overview

Features at glance

- Fully controlled and configured over open-standard Wishbone Interface
- Uses open-source PCI Wishbone from OpenCores.org, GNU LGPL
- SLR in pure VHDL and Verilog source code ⇨FPGAs from any vendor might be used
- Time critical 2KHz operations into hardware
- Uses multiple clocks derived from H-maser
- Enables use of SLR frequencies up to 10KHz
- Free Ie's ⇨further extensions
- CycloneII/III FPGAs ⇨old enough ⇨free Altera Quartus 9.x Web Edition ☺
- Own Windows and linux driver for the board

SLR FPGA description

Functionality

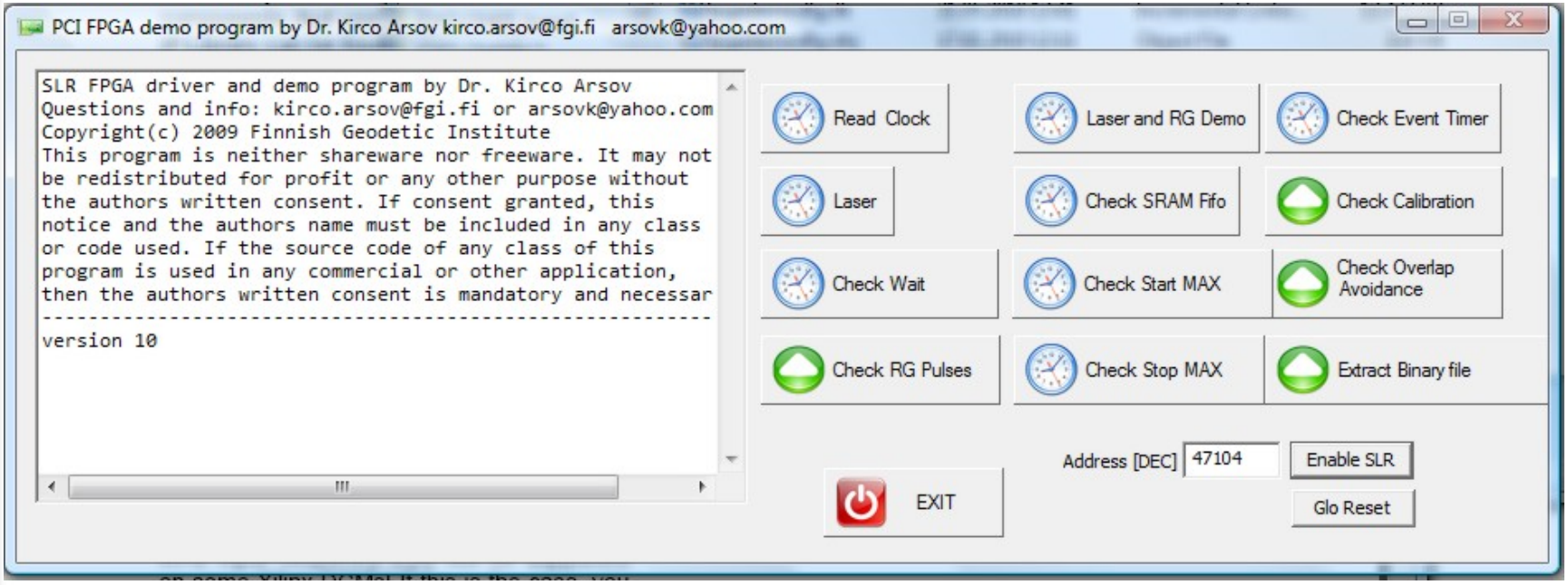
- Manage the Range Gate pulses
- Integer and fractional part of the expected RG is written in the PCI registry sent to the C-SPAD
- FIFO of 1024 points is used inside the board
- Controlling of the laser fire frequency
- user might change on-the-fly the laser frequency
- Calibration and CCD control is programmed, and is fully automatic
- Event timing with 5ns resolution
- Start as well as stop events are time-stamped and put into 1024 FIFOs

SLR FPGA description

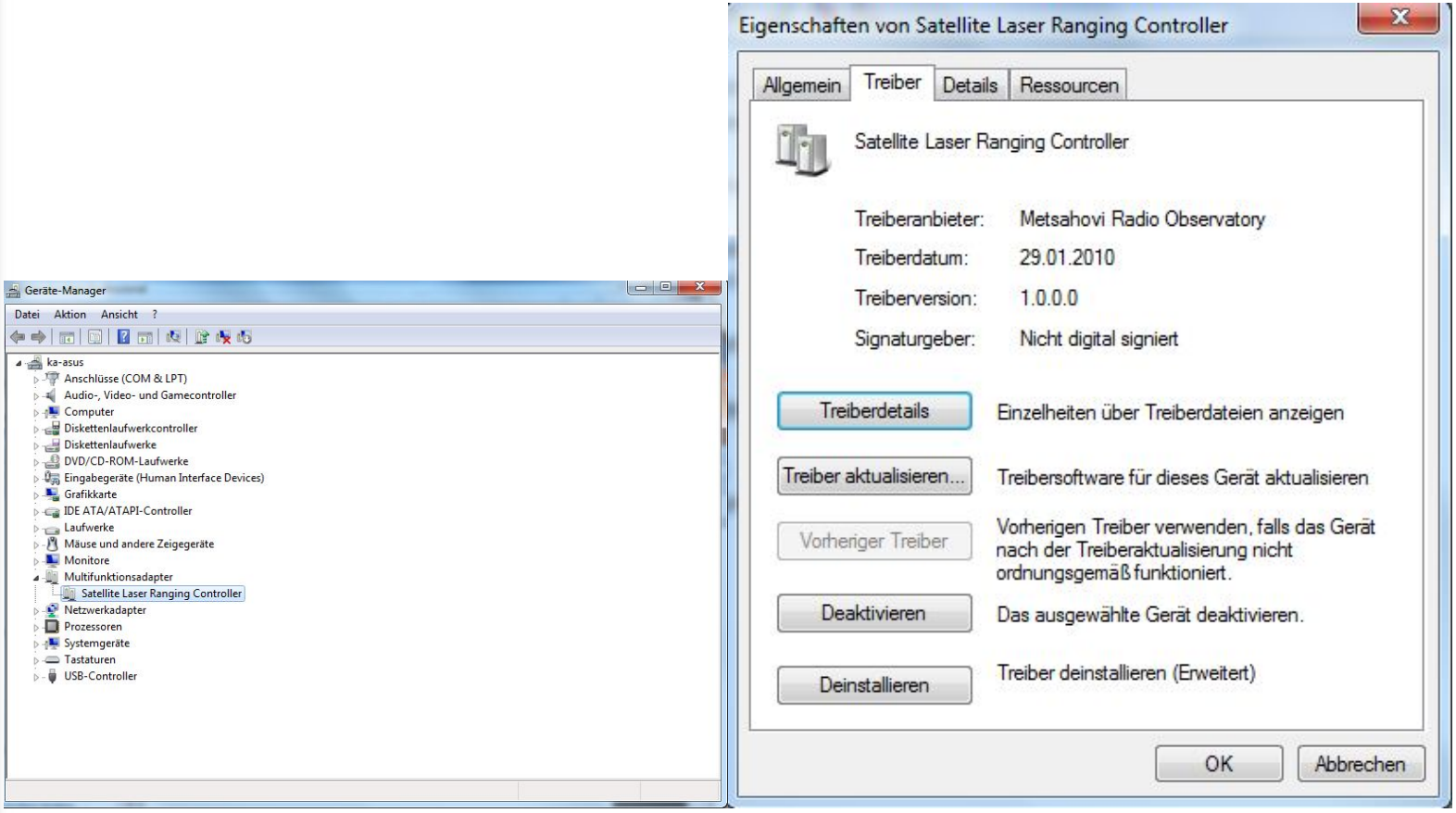
Functionality

- Integer and fractional part, so absolute reading is possible
- Couple of counters readable, 10MHZ and 200MHz
- Implemented overlapping avoidance of start and stop signals and the user might adjust on-the-fly the intervals of overlapping
- Calibration mode as well as CCD mode fully automatic
- Fully implemented into our SLR software
- Demo program to test the functionality of the board

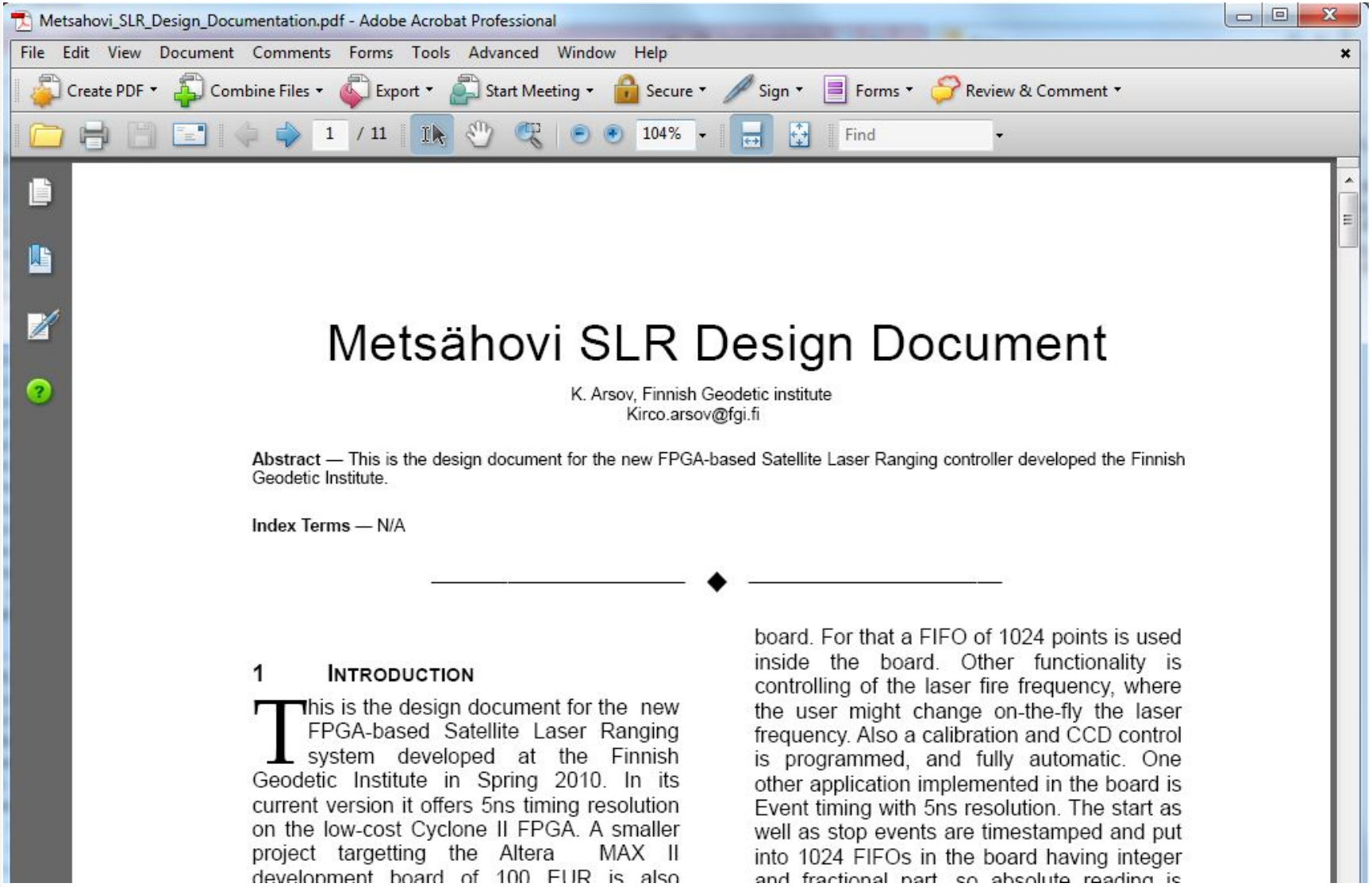
Demo program for board functionality test



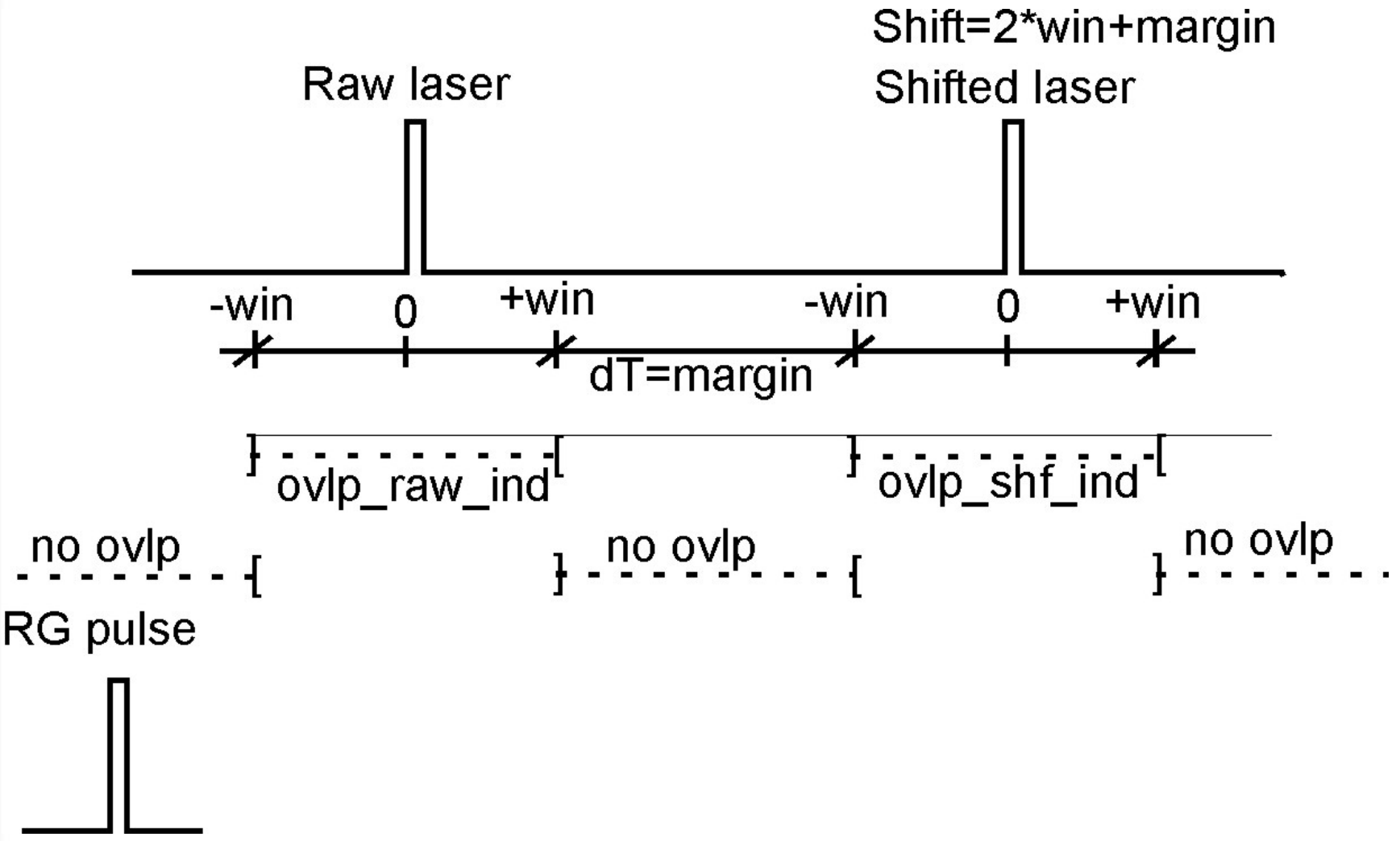
Windows and Linux drivers programmed



Project documentation



Note on OA


Shift=2*win+margin
Raw laser
Shifted laser
-win
0
+win
-win
0
+win
dT=margin
ovlp_raw_ind
ovlp_shf_ind
no ovlp
no ovlp
no ovlp
RG pulse

OA verilog comments

```
// Description: Laser pwm and range gate pulses as input.
//
// Outputs a shifted laser pwm signal that
// attempts to avoid overlap of laser and range gate.
//
// Attempts to keep the rising(!) edges of the laser
// at a certain minimum distance away from range gate
// pulses. The window is symmetric, laser to RG
// and RG to laser edge time deltas are kept
// longer than the window time by adjusting the
// laser phase shift when it seems that laser/RG
// are too close.
//
// Adjustment method: overlap of direct Laser pwm and a
// fixed-delay (2*window+T) Laser pwm versus Range gate
// is monitored. If direct pwm indicates overlap,
// we output the fixed-delay pwm. And vice versa.
```

OA verilog comments

```
//
// Does NOT act based on the _current_ range gate
// target. The time deltas are always taken from
// the latest pulses already output.
//
// Note: the pulses are allowed to overlap in
// time e.g. when pulse widths or duty cycle are long.
// Only the rising edges are not allowed to be too close.
//
//  output <= Raw_Laser when overlap_shifted_ind=='1' else
//            Shifted_Laser when overlap_raw_ind=='1' else
//            WhateverWasSelectedLastTime;
//
```

And very important...

IT IS FREE TO ANYONE INTERESTED!!

(GPL) licence; FPGA Verilog + Demo Code freely available to SLR community!

That's all folks...

THANK YOU

FOR YOUR ATTENTION

Questions?

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