Medium Resolution Digital Event Timer and Range Gate Generator in Graz FPGA Card

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Abstract

For our kHz Satellite Laser Ranging (SLR) system in Graz, we developed a fast response, medium resolution Event Timer to determine laser firing times; and a digital Range Gate Generator to activate the Single Photon Avalanche Detector (C-SPAD). The Event Timer has a resolution of 250 ps, and determines the Event Times within 20 ns; the Range Gate Generator produces a range gate pulse with 500 ps resolution, and better than 1 ns accuracy. Both devices are fully digital, and are implemented within an FPGA circuit. These devices can be used in the present 2 kHz SLR system, as well as in future higher repetition rate SLR systems.

Introduction

An SLR system consists of a laser, a telescope, a – single or multiple - photon detector (in Graz: C-SPAD) and a time of flight (TOF) measurement device. The TOF can be measured with 2 different methods: With a simple time interval counter, or with event timers.

Time interval counters are not applicable for kHz SLR, because due to the high repetition rate (some kHz) there are always more than 1 pulse – up to 300 pulses for high orbit satellites for a 2 kHz SLR system – simultaneously traveling between SLR station and satellite.

Event timers determine laser firing epochs and epochs of the returns independently; these epochs are used to calculate the TOF. Because the ultra high precision Graz E.T. (< 2.5 ps) needs about 400 µs to fix the event time (Kirchner et al, 2000), we developed a much faster (20 ns response time), but medium resolution (250 ps) event timer within the FPGA, dedicated – and accurate enough - for range gating purposes.

Figure 1. Graz ISA PC Card; FPGA containing Event Timer and Range Gate Generator

After detecting a laser start pulse event time, the expected return event time is calculated, and loaded into the Range Gate Generator; which then activates the detector short before arrival of the return photon(s). While this is done at present with a combination of a digital 100-ns-resolution FPGA counter PLUS a programmable analog delay chip, we implemented now a fully digital Range Gate Generator into the FPGA - using a 5-ns-course counter, and a 500 ps vernier – to improve linearity and stability.

Both devices were implemented within the Altera FPGA Apex 20K chip on the Graz FPGA card (fig. 1).

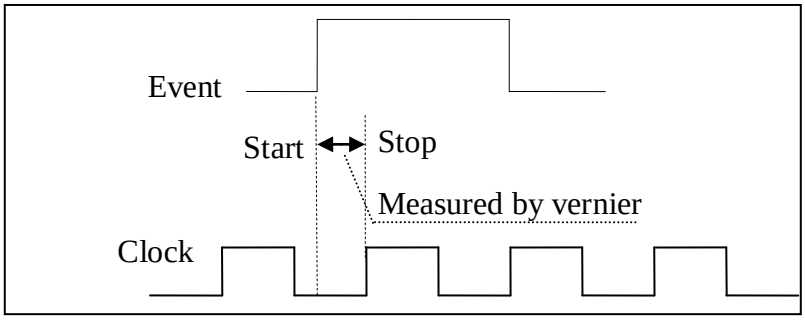

Figure 2. A digital vernier interpolates between 5 ns clock pulses.

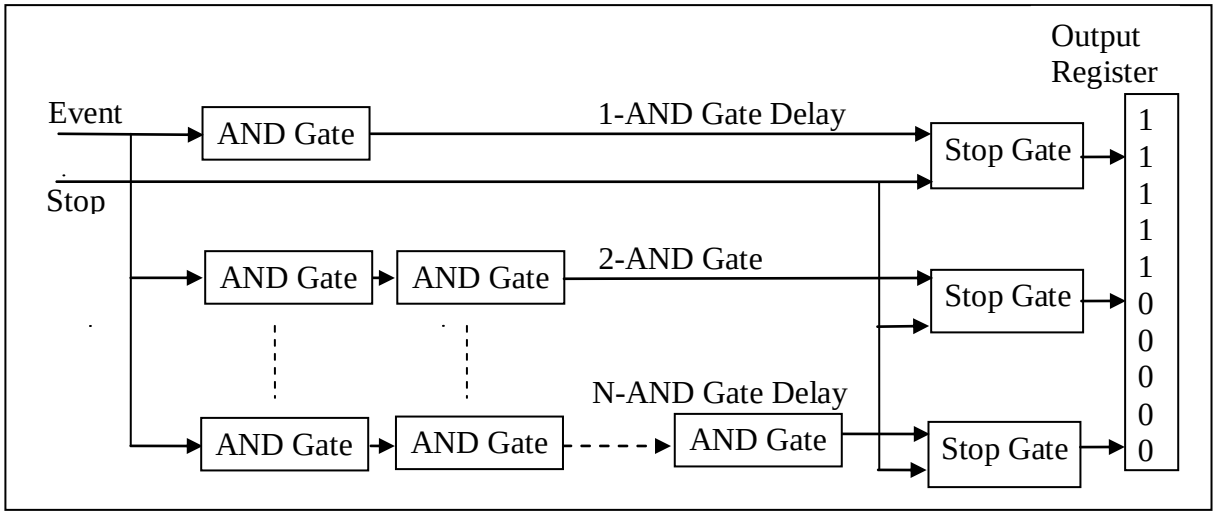

Figure 3. Event timer unit, using chains of AND delay gates of increasing length.

Event Timer Implementation

The fast response digital event timer is implemented using a well known vernier method. This method uses a 200 MHz counter and a vernier for the 5 ns intervals. The vernier uses standard AND gates with 250 ps transit time per gate (fig. 2). To implement a series of identical, cascaded delay gates we had to disable the automatic optimization of the Quartus Compiler for the Altera FPGA device.

The event pulse (e.g. Laser Start Pulse) starts traveling through several parallel chains of AND Gates; each chain consists of an increasing number of AND gates; the next following 5 ns clock pulse is used as a STOP pulse for this simple vernier (fig. 4). If the start pulse

reaches the end of a chain BEFORE the STOP pulse, a "1" is latched into an output register; if not: a "0"… (Fig. 3). The bits in this output register represent a measure for the 0-5 ns interpolation; together with the latched actual reading of the 200 MHz coarse clock this forms a 250 ps resolution event time.

We implemented this event timer into the Graz ISA card FPGA and optimized its floor plan layout to achieve best linearity and uniform resolution. Simulation of such a circuitry gives promising results for the required speed and resolution of this Event Timer (fig. 4).

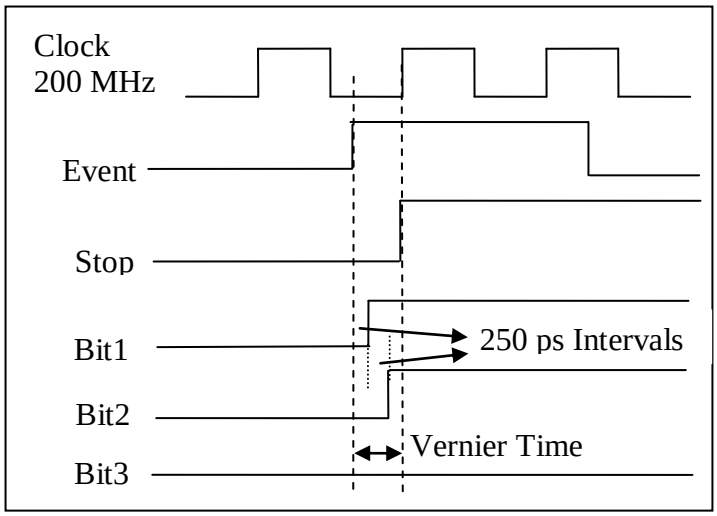

Figure 4. (A) Vernier measurement, interpolating 5 ns intervals.

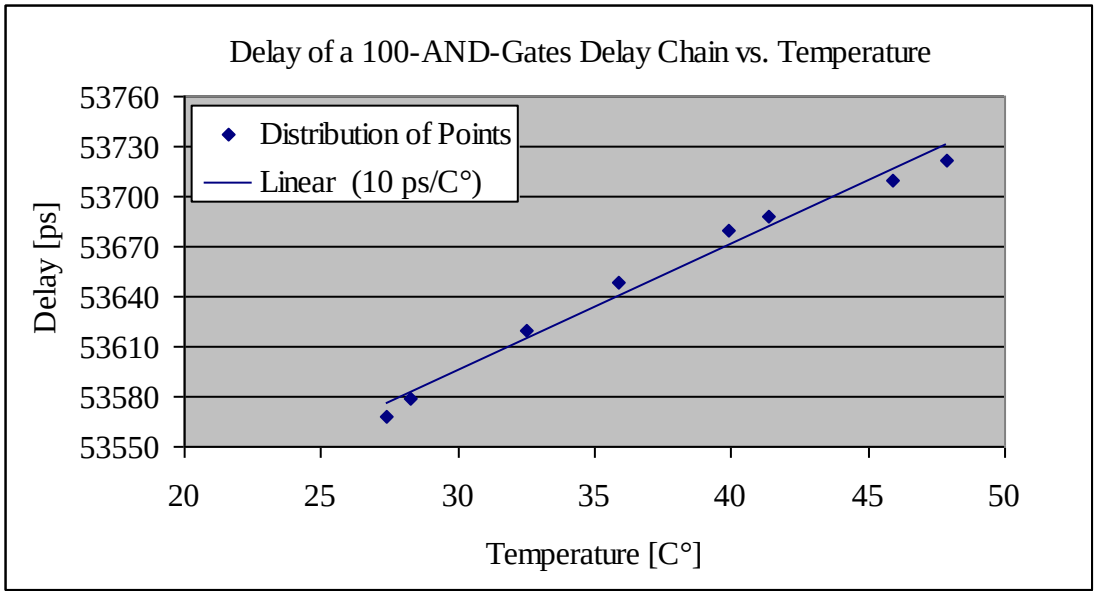

Figure 5. Delay of a 100-AND-Gates Delay Chain vs. Temperature.

Event Timer Experiment and Conclusions

We tested the temperature drift of a 100-AND-gate delay chain; it drifted with about 10 ps/C° (Fig. 5), which is quite acceptable considering the required resolution, and the location of the PC / ISA Card / FPGA in the air conditioned laser room.

To evaluate the FPGA event timer linearity, (fig 6: Test setup) we compared its results with those of our ultra high precision (1.2 ps resolution, < 2.5 ps non-linearity) Graz E.T. (Kirchner et al, 2004). The differences between both showed an RMS of 260 - 290 ps(fig.7).

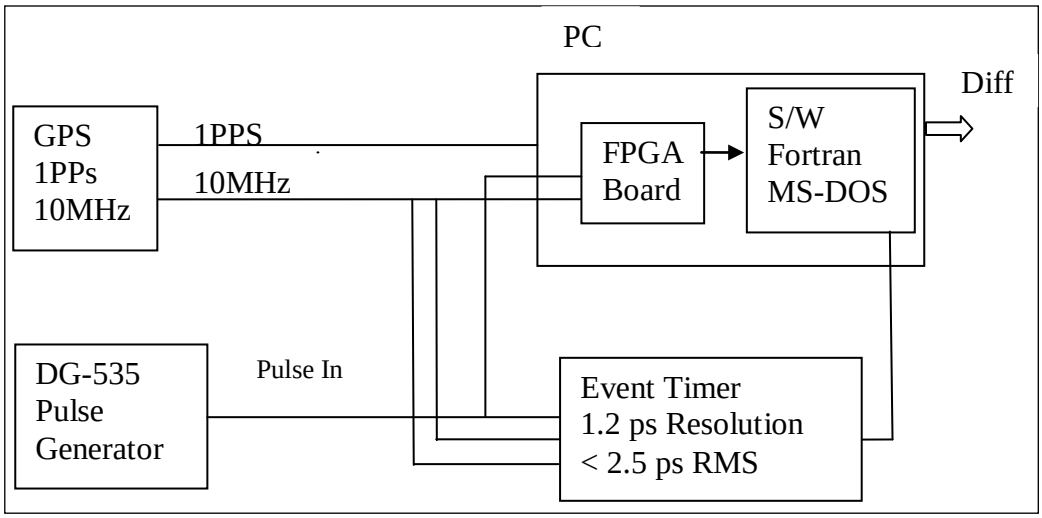

Figure 6. Test setup to compare Graz E.T. and FPGA ET measurements

Although an event timing accuracy of < 300 ps is fully sufficient for the purpose of Range Gate Epoch determination, we tested possible improvements by implementing 4 such Event Timer Units in parallel (**fig** 7) into the FPGA. All 4 event times are read by PC and averaged there; this average reduces the FPGA event timer jitter to 217 ps RMS (fig. 8).

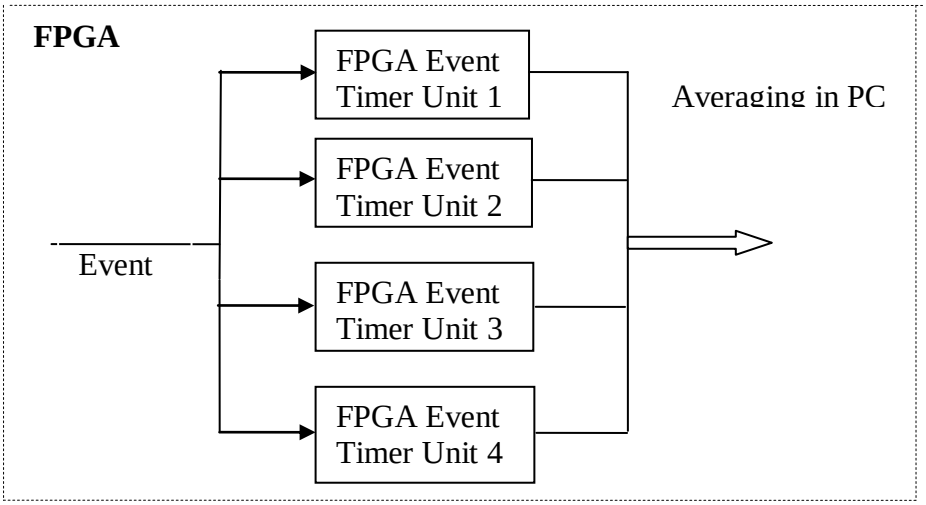

Figure 7. 4 Parallel Event Timers.

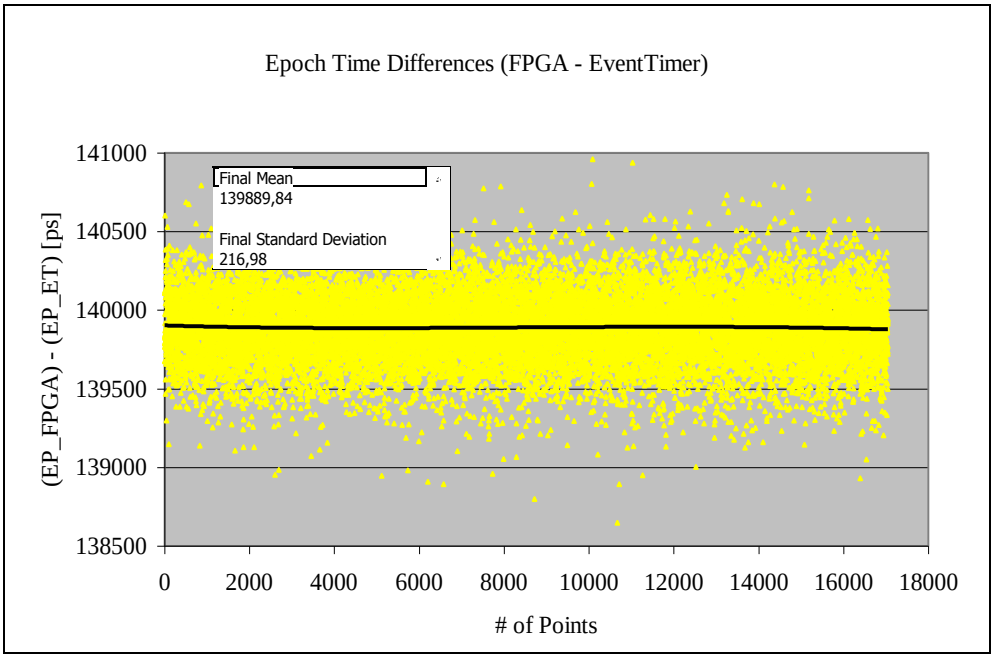

Figure 8. 4 Parallel Event Timers: Standard deviation of 217 ps

Conclusion: Resolution and non-linearity of a single FPGA Event Timer unit is more than adequate for our purpose; for even better resolution, a multi-channel Event Timer can be implemented. Due to its very high speed, it is well suited for the existing 2 kHz SLR system and also for systems with significantly higher repetition rates.

Range Gate Generator

We used a 200MHz clock and a chain of AND gates to implement a Range Gate Generator (programmed via PC) - which generates a range gate pulse short before the actual return of the laser photons - with a resolution of 500 ps and an accuracy of < 1ns.

The start pulse (fig.8) travels through the chain of AND gates. The output of each gate switches its associated D-Flip-Flop as soon as the start pulse has passed; only ONE out of these D-Flip-Flops is activated by the pre-programmable selection logic, and generates the Range Gate pulse (fig. 9).

Experiments and Conclusions

We implemented a test setup using a DG535 Pulse Generator, a Stanford SR620 Time Interval Counter, and a GPS system (1 pps) to test the linearity of the Range Gate Generator.

We tried 3 different placements (floor plan layouts; both manual placements and/or automatical placements of the AND gates and D-Flip-Flops within the logical cells) of the Range Gate circuitry inside the FPGA to find the optimum linearity (Fig.10); the selected final placement has the best R-squared value ("R2" in fig. 10) and linearity.

Conclusion: The Graz ISA PC Card with FPGA now contains also a 250-ps resolution event timer and a fully digital Range Gate Generator. Both are used to speed up the RG setting for present 2KHZ SLR systems.

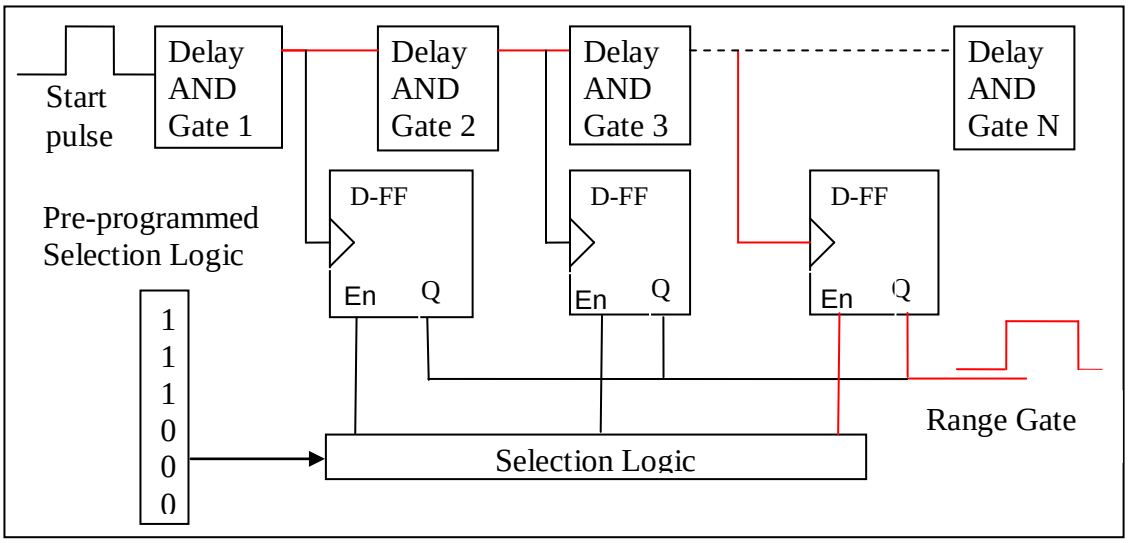

Figure 9. Block Diagram of Digital Range Gate Generator.

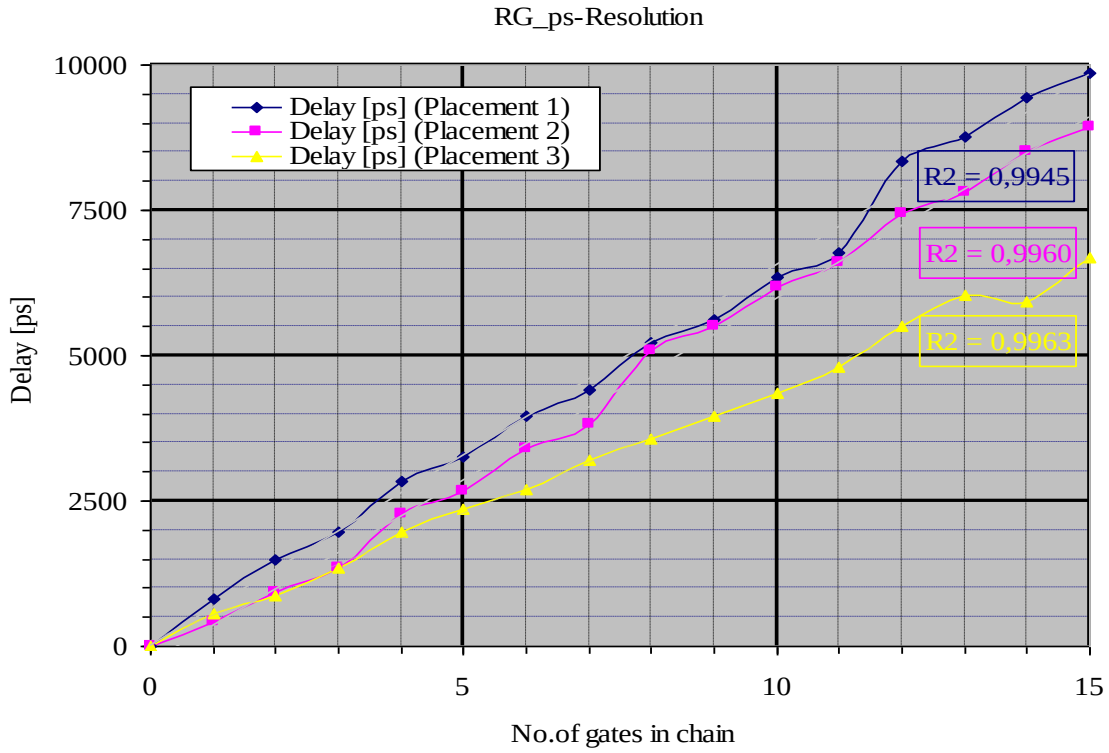

Figure 10. Delay Time (ps) vs. Delay Chain Length – different placements of AND gates and D-Flip-Flops to optimize linearity.

References

Kirchner G., Koidl F. (2000): *Graz Event Timing System;* Proceedings of 14th Int. Workshop on Laser Ranging, Matera, Italy.

Kirchner G., Koidl F. (2004): *Graz kHz SLR system: Design, Experiences and Results* Proceedings of 14th Int. Workshop on Laser Ranging, San Fernando / Spain.