Upgrading of Integration of Time to Digit Converter on a Single FPGA

Young ZHANG[1,2], Peicheng HUANG[1] and Renjie ZHU[1,2]

[1]Shanghai Astronomy Observatory, Chinese Academy of Sciences,

80 Nan Dan Road, Shanghai, China 200030

[2]Graduate School of the Chinese Academy of Sciences, 19A Yu Quan Road, Beijing, China 100039

zhang.young@gmail.com, pchuang@shao.ac.cn & zhurj@shao.ac.cn

***Abstract*-A Time to Digit Converter (TDC), which can achieve resolution 50-60 picoseconds, is integrated on a single FPGA. Implementation a TDC on FPGA provides not only higher precision and shorter dead time compared to traditional methods，but also higher scale of integration. As the system can be integrated into single chip, it is especially suitable for portable and satellite-borne system. Besides, the resolution is expected to be improved to less than 30 picoseconds. Principle of operation, architecture of the prototype, the construction of this TDC and the nonlinearity are presented in this paper.**

I. INTRODUCTION

Traditional high-precision time interval measurement techniques include time stretching method, time-to-amplitude method and Vernier method, tapped delay line method and differential delay line method [1]. There were two examples to integrate TDC on a single FPGA. Jozef Kalisz et al adopted differential delay line method on QuickLogic's pASIC2 FPGA, which achieved 100 ps LSB [2]. Zielinski and Chaberski, using tapped delay line method, implemented a module on Xilinx's XCV300 with 100 ps resolution [3]. In this paper, a TDC is implemented on XC4VSX35 FPGA with 50-60 picoseconds resolution.

Table I lists main parameters of this module.

II. GENERAL DESIGN

A. Interpolating Principle

Interpolating methods are widely used because of its advantages in both long measurement range and high resolution. With interpolating methods, a time interval T generally consists of three parts. A major part, nT_p, is measured in real time by reference clock. The remaining two short intervals ΔT_1 and ΔT_2 are defined at the beginning and at the end of time interval T, which are measured by insulators. In this design, they are measured by two tapped delay lines. Fig. 1 gives the math relation between them.

TABLE I DESIGN SUMMARY

Standard uncertainty	50--60 picoseconds
Resolution/LSB	50--60 picoseconds
Measurement Range	0-99999 seconds
Input Reference Clock	10MHz Rb Atom Clock
Calibration Mode	Real time Calibration

B. Reference clock

The input 10MHz reference clock from Rb atom clock is quite stable but not high enough for interpolating. With built-in DCM on FPGA, it is synthesized into 200MHz. As shown in Fig.1, the time interval nT_p is counted by the reference clock 200MHz. The measurement jitter of 200MHz reference clock is about 60 picoseconds.

C. Tapped Delay line

The tapped delay line is made of slices--the basic unit of Virtex FPGA. As shown in Fig.2, a delay unit and a D flip-flop, is in the dashed line. The dashed part of delay logic can be implemented in a single slice, as shown in Fig. 3. These slices cascade

to form a slice chain, i.e., a tapped delay line. Two delay lines of this kind, measure the short time interval ΔT_1 and ΔT_2 respectively.

The delay unit of slice utilizes the fastest path, fast carry logic, to obtain the highest resolution. It's assumed that all delay units are of the same delay time τ. The measurement average delay τ, which determines the resolution or least significant bit of this module, is about 50-60 ps. However, this assumption does not fit the facts perfectly. The nonlinearity of the tapped delay line is measured and analyzed in part III.

III. MEASUREMENT DATA

In this part, the measurement data of this module is compared with those of SRS's SR620. To demonstrate the resolution of this high-precision TDC, y axis of Fig 4 is marked with TDC measurement, while the x axis is marked with SR620 measurement.

The difference between two groups of measurement, which is equal to the differential nonlinearity, is given in Fig. 5. In Fig.5, the maximum difference is about 300 picoseconds. The difference measurement can be repeated in other time cycle, which means it can be corrected with prior knowledge of it. This will be part of further research. Besides, with a little internal modification, the resolution is expected to reduce to less than 30 picoseconds, which means 50 % improvement in resolution.

Fig.6 is a snapshot of our measurement experiment.

REFERENCES

[1] Józef Kalisz. Review of methods for time interval measurements with picosecond resolution Institute of Physics Publishing Metrologia, vol 41 pp17～32. 2004

[2] Szplet R, Kalisz J and Szymanowski R. Interpolating time counter with 100 ps resolution on a single FPGA device IEEE Trans. Instrum. Meas. vol 49 pp.879–883, 2000

[3] Zielinski M, Chaberski D and Grzelak S 2003 Time-interval measuring module with short dead-time *Metrol. Meas. Syst.* 10.

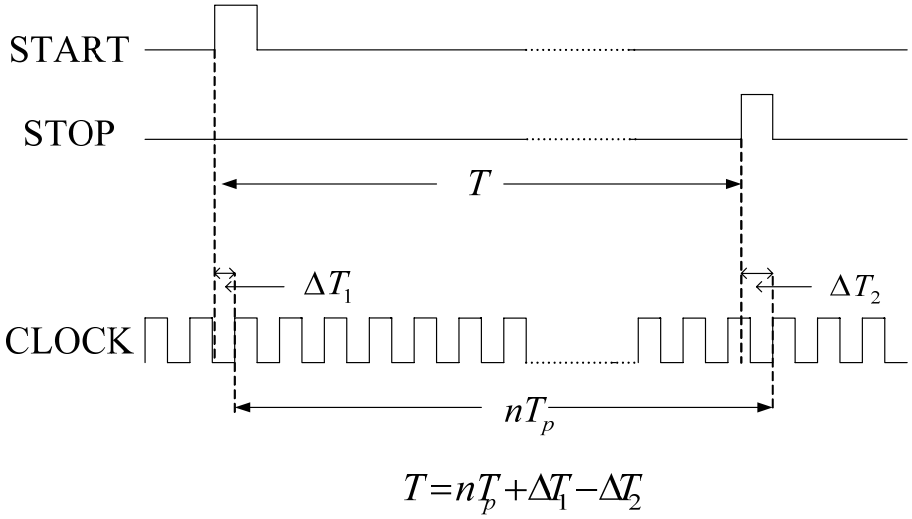

Figure 1. Interpolating Principle

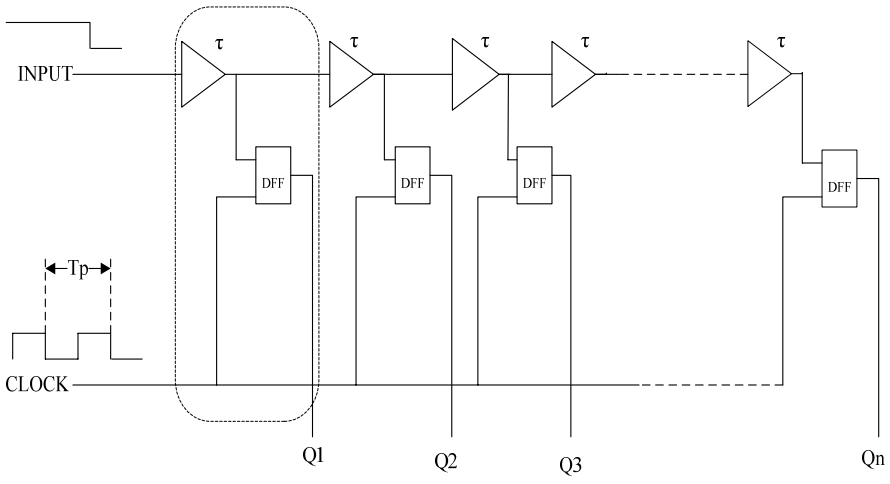

Figure 2. Tapped delay line made of slices.

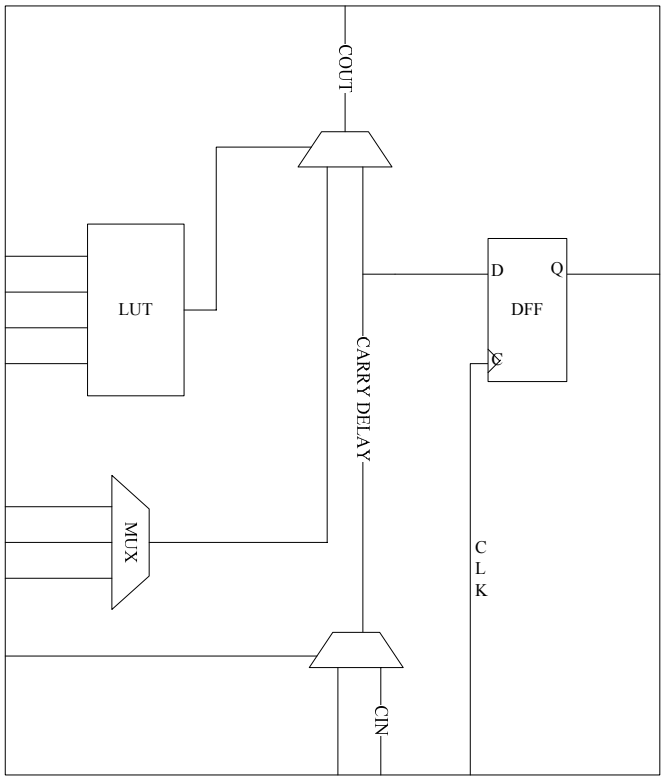

Figure 3. Simplified slice configuration as delay unit.

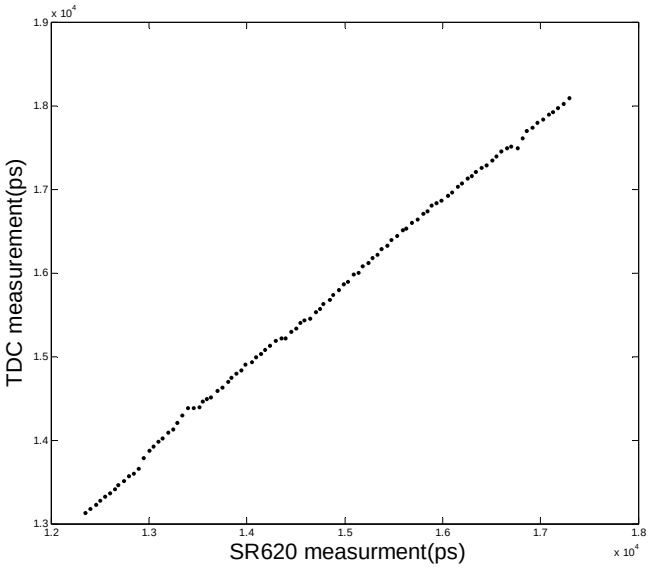

Figure 4. Comparison of TDC measurement with SR620 measurement

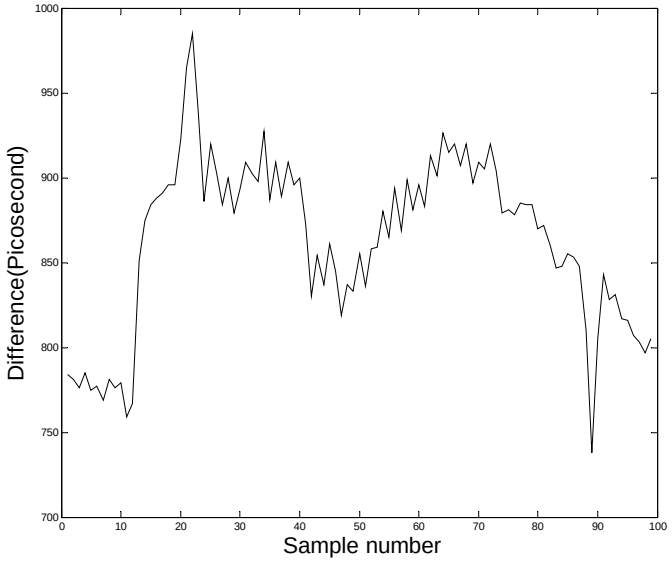

Figure 5. Difference between TDC and SR620

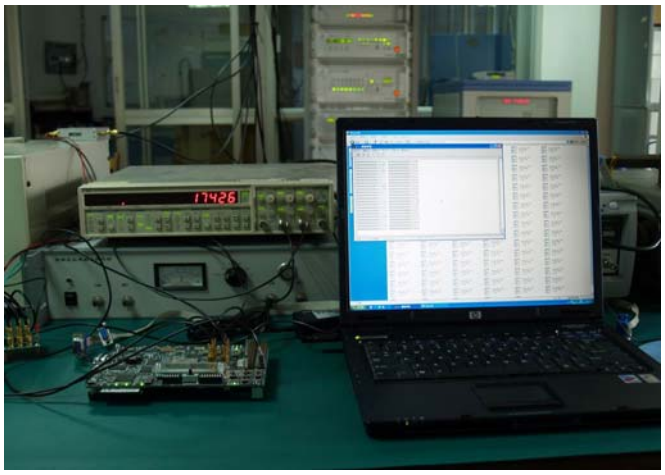

Figure 6. Measurement experiment