

The KHz Ranging Engine (KRE)

V1.2 Description

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Introduction

Metal Tech and NiCT have developed a KHz-capable ranging controller, principally for upgrading the SLR systems at Koganei as future path.

Key Conceptual Features:

- functionality in a variety of environments
- access to source
- modern and compact
- field upgradeable

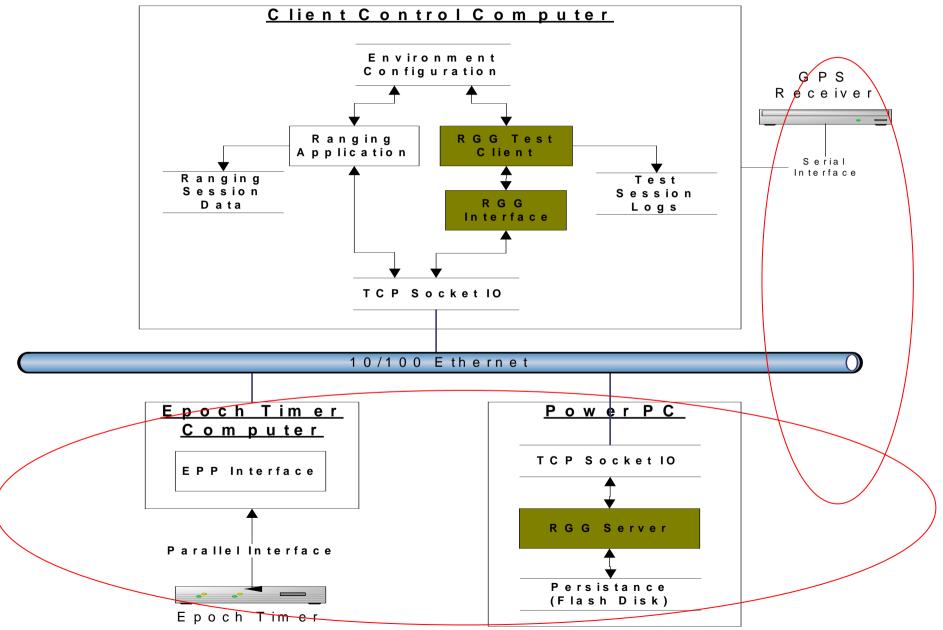
KRE Looks :



General Features

- One box with RGG (range gate generator) and A032ET servers.
- Separate 100BaseT LAN communications to each server.
- 2U high, 19" rack-mounting package.
- 100~250VAC 45~65Hz, 1Φ.
- Warm reset functions.
- TCP/IP communications.

Block diagram :Communications



RGG Server Features 1 of 4

- Implementation platform XILINX V4Fx12, test C software implemented in Virtex Power PC
- On-board multipliers and dividers, 500MHz base frequency, 2ns granularity on all signals
- Precision frequency inputs: 10MHz 1pps
- Signal outputs:

buffered 10MHz, 1MHz, 1pps (square) 6 sequential triggers at laser fire time (TTL) 2 range gates, config. widths & delays (NIM)

RGG Server Features 2 of 4

- Epoch (1pps) outputs are synchronized to UTC independent of display time.
- On-board linear interpolation of blocks of range information.
- On-board collision avoidance via laser fire delay register.
- RS232 serial port for diagnostic data FIFO service task runs at 200Hz

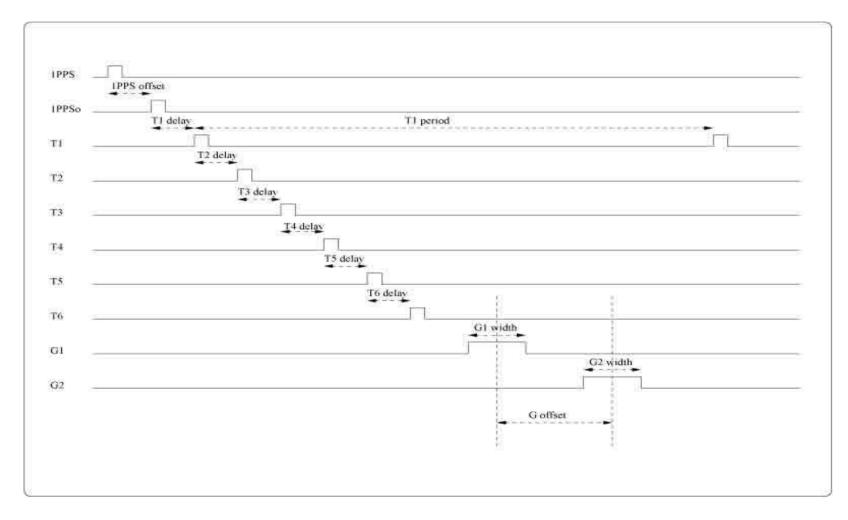
RGG Server Features 3 of 4

- Range gates are epoch triggered
- The RGG is a sequential device, where randomness should enter via jitter in laser fire.
- No limitations to a multi-stop environment.
- Any PRF from 1Hz to 2KHz

RGG Server Features 4 of 4

- Interpolation is always on. Range rate is determined on board.
- Collision avoidance is always on.
- Gates are epoch triggered, no matter the range.
- The purpose of the two range gates is to deal with old style MCP detectors that require significant settle time after being gated on.

Timing Chart: Triggers andRange Gate signals1 of 1



Short, fixed range 1 of 1



Moving Target 1 of 1 Collision band handling



Top trace is Gate1 Bottom trace is laser fire

'scope persistence is on

ET Server Features 1 of 1

- Primary purpose is to handle the A032ET device
- Implemented on single-board PC under Linux, 60GB hard disk
- Bandwidth can run Latvian demo mode 1 at ≥10KHz
- On-board USB2.0 port accessible via server software, used for Rx controls, such as: shutters OD LC filter
- H-Interface implemented on Java machine support DHCP, Ping, Telnet and FTP

Collision Band handling : Efficiency

- Collision zones are handled by a parameter controlling the allowable separation of laser fire and gate open. For the duration of the overlap, the laser fire signal is delayed, with the effect of reducing PRF.
- The following table show testing not exhaustive, but indicative of performance.

Collision Band handling Efficiency

PRF Hz	Range	Gate ns	Collision Deadband	%
.1K	1~42ms	76	30 µs	>97
1K	1~42ms	76	30 µs	>95
2K	1~42ms	500	65 µs	>90
2K	150ns	76	30 ns	99.9
1K	.1~1.09s	76	30 µs	>95
2K	.1~1.09s	500	65 µs	>90
2K	2.6~2.7s	500	65 µs	>90

Limitations 1 of 2

 FIFO depth is 6000 which limits the maximum range wrt PRF and gates:

PRF	Max Range with Gates		
	1or 2	1 & 2	
2KHz	3 sec	1.5 sec	
1 KHz	6 sec	3 sec	
500Hz	12 sec	6 sec	

Limitations

 Increasing FIFO size requires reorganization of internal Xilinx memory.

FIFO depth is 6000 which limits the maximum range wrt PRF and gates, can do 2kHz Lunar Ranging but not Planetary.

- The RGG does not understand change of year.
- Range gate minimum width is 76ns.
- The Riga ET in Mode 1 can deal with one start and stop event. A multi-stop environment will require <u>an ET server for each stop</u>.
- Internal cals can only be done with fixed-range targets.

Conclusions

- We have created a very versatile device with few real limitations, off-loading many tedious functions from a client control computer.
- Only special PCB is for signal distribution, other devices are commercial products.
- The brains are in the VHDL firmware and software, so logic updates can be flexible for new requirement.

Acknowledgements

- The on-board hardware delay design for collision avoidance is based on ideas discussed at Graz in 2004.
- Clever contractors:

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