Sub-picosecond event timing
new techniques & first results

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New timing principle theory by Petr Panek
## US Patent, 2005

Petr Pánek was born in Rakovník, Czech Republic, in 1957. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Czech Technical University, Prague, Czech Republic, in 1982 and 1988, respectively.

From 1986 to 1988 he was with Aeronautical Research and Test Institute, Prague. In 1988 he joined Mesit, Uherské Hradiště, and since 1993 he has been with Dicom, Uherské Hradiště as a Senior Research Engineer responsible for positioning and timing systems. Since 2004 he is also a scientist at the Institute of Radio Engineering and Electronics, Academy of Sciences of the Czech Republic, Prague. His current research interests are accurate time transfer and time interval measurement.

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Design Goals

- Sub – picosecond event timing device

- Based on novel timing principle (P.Panek)

- Employing new technologies
  (ultrafast logic, "no ground", SAW filters,..)

- Self - calibrating device
  no adjustment or calibration needed ever

- Space version possible (low mass, low power,..?)

Operating principle
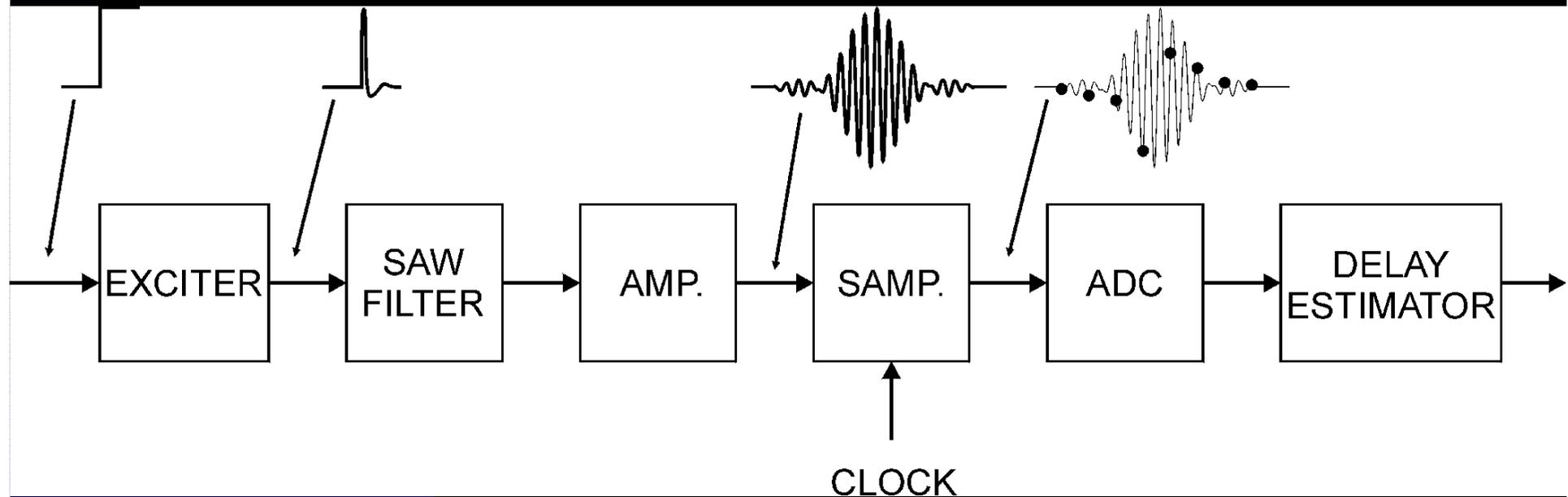
- The entire time measurement is carried out in a FREQUENCY DOMAIN

- The time-interpolator is realized by the Surface Acoustic Wave SAW filter

- The SAW filter output is sampled & digitized synchronously with the clock

- The resulting time / epoch is computed using the reverse FFT

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Data processing

Popis algoritmu:

1. Meze intervalu, na němž hledáme maximum, položíme $s_1 = -2, s_2 = 2$ a počáteční odhad $s = 0$.

2. Určíme velikost korelace v bodě s_1

$$r_1 = \left| \sum_{k=1}^{31} R(k) \exp\left(jks_1 \frac{2\pi}{64} \right) \right|.$$

Výpočet provedeme následujícím způsobem:

$$C_1(k) = \cos(ks_1\pi/32),\ S_1(k) = \sin(ks_1\pi/32),\ k = 1,...,31,$$

$$\mathrm{Re}[a_1] = \sum_{k=1}^{31} (\mathrm{Re}[R(k)] \cdot C_1(k) - \mathrm{Im}[R(k)] \cdot S_1(k)),$$

$$\mathrm{Im}[a_1] = \sum_{k=1}^{31} (\mathrm{Re}[R(k)] \cdot S_1(k) + \mathrm{Im}[R(k)] \cdot C_1(k)),$$

$$r_1 = \sqrt{\mathrm{Re}[a_1]^2 + \mathrm{Im}[a_1]^2}.$$

3. Určíme velikost korelace v bodě s_2

$$r_2 = \left| \sum_{k=1}^{31} R(k) \exp\left(jks_2 \frac{2\pi}{64} \right) \right|.$$

Výpočet provedeme následujícím způsobem:

$$C_2(k) = \cos(ks_2\pi/32),\ S_2(k) = \sin(ks_2\pi/32),\ k = 1,...,31,$$

$$\mathrm{Re}[a_2] = \sum_{k=1}^{31} (\mathrm{Re}[R(k)] \cdot C_2(k) - \mathrm{Im}[R(k)] \cdot S_2(k)),$$

$$\mathrm{Im}[a_2] = \sum_{k=1}^{31} (\mathrm{Re}[R(k)] \cdot S_2(k) + \mathrm{Im}[R(k)] \cdot C_2(k)),$$

$$r_2 = \sqrt{\mathrm{Re}[a_2]^2 + \mathrm{Im}[a_2]^2}.$$

4. Určíme velikost korelace v bodě s

$$r = \left| \sum_{k=1}^{31} R(k) \exp\left(jks \frac{2\pi}{64} \right) \right|.$$

- Purpose – converting the sampled and digitized wavefronts data into epochs

- Recursive ("selflearning") algorithm dedicated for repeated measurements

- The device self-calibration is included

- Complicated algorithm consisting of a numer of compex double precision arrays manipulation, multiple FFT etc.

- See attached list for ~ 10% of the description ☺

- High CPU and data volume requirements Time consuming, repetition rate limit ☹

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Device design

- Based on theoretical papers by P.Panek, submitted to IEEE 2004-5

- Selected optimal combination of SAW filter central frequency, bandwidth, ...

- Based entirely on commercial components (2005)

- The clock reference – 200 MHz Frequency Module designed and constructed by J.Kolbl and P.Sperber, Univ. of Deggendorf, 2005

- On the input stage employed the fastest available components,

- The device designed as modular, two channel event timer to enable independent modules modification and upgrade

# Device construction
Event timer in operational configuration
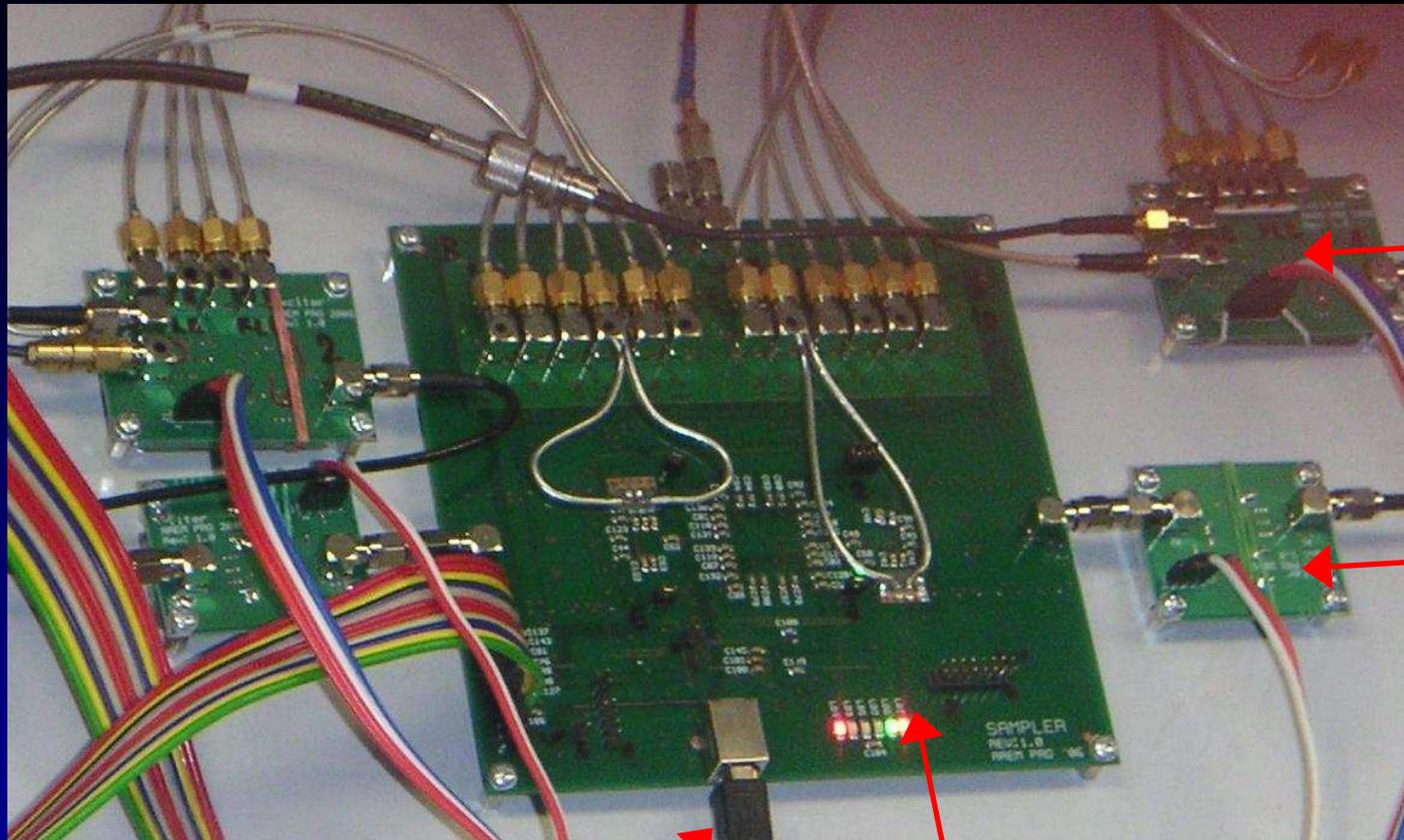
Exciter

SAW filter

USB 2

Sampler and AD converter

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Technology challenges
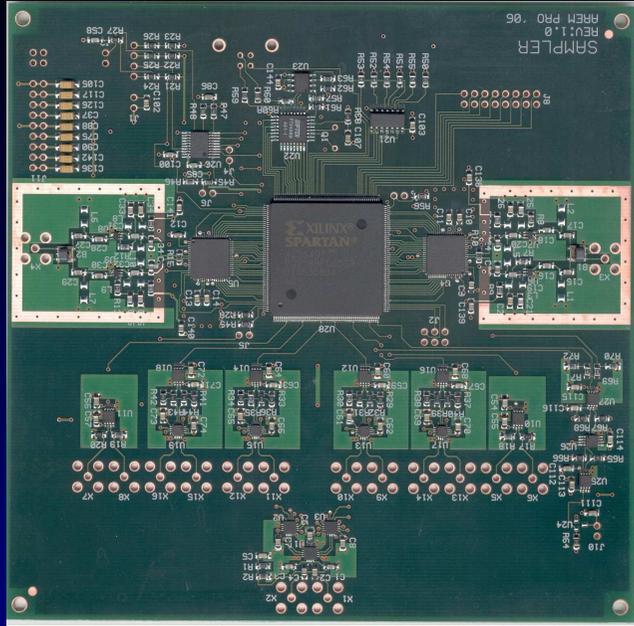
- PCB design
  Advaced PCB design SW
  crashed due to board complexity ☺

- Equal signal path delay requirement
  (PCB + cable + PCB) < 10 ps   (!!)

- On board micro-strip ps delay lines

- Sub - mm cable length tolerances (!!)

- Soldering of some SMD chips

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200MHz clock source
J.Kolbl and P.Sperber, Univ. of Deggendorf
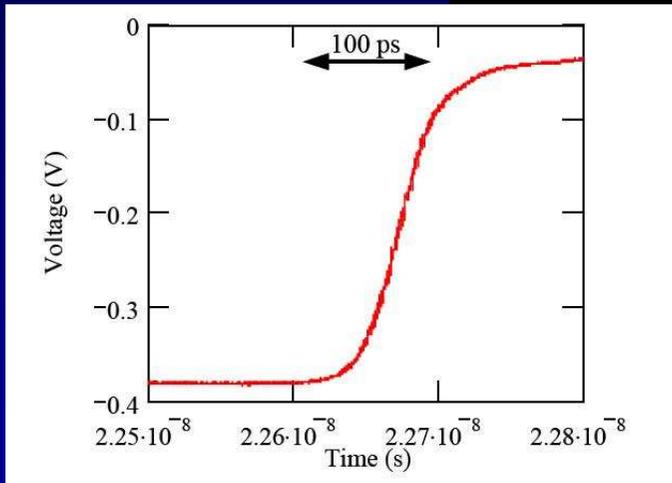
Risetime < 40 ps

Clock jitter << 1 psec

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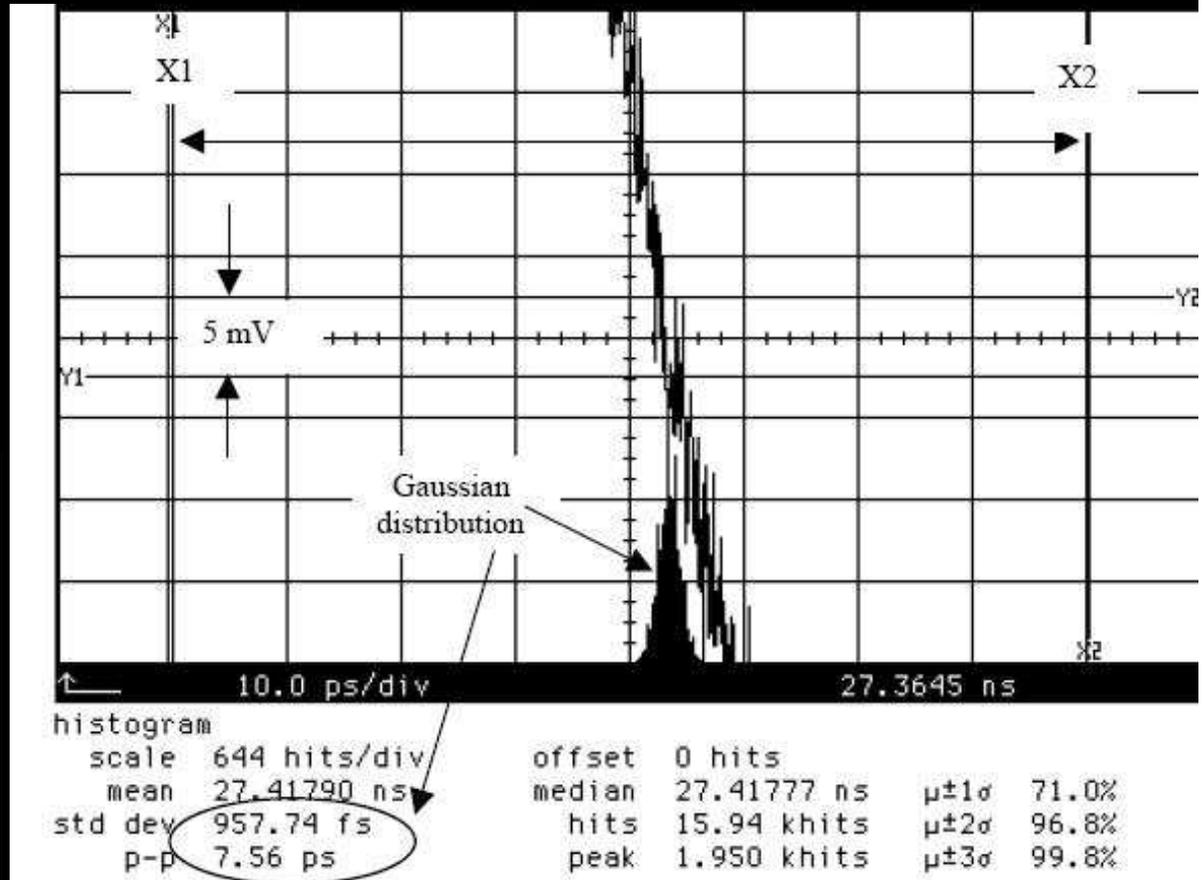
Device construction
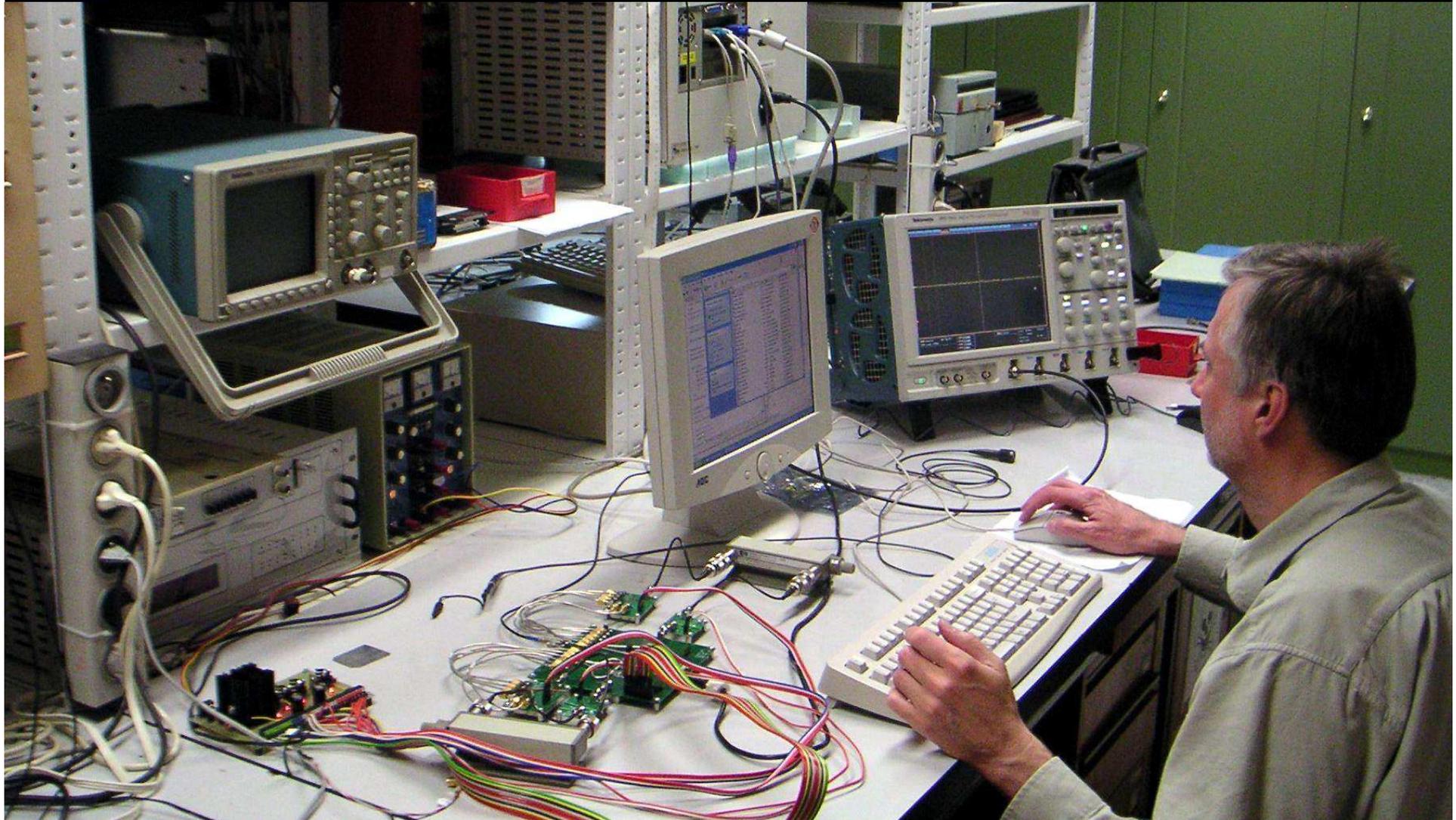
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Random error budget - individual contributors

	rms ps / channel
Noise of excitation	0.78 ps
Noise of amplifiers	0.29 ps
Quantization	negligible
Clock and sampling jitter	0.30 ps
Aliasing	0.35 ps
Resulting root sum square	**0.95 ps rms / ch**

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Timing jitter - cable delay test
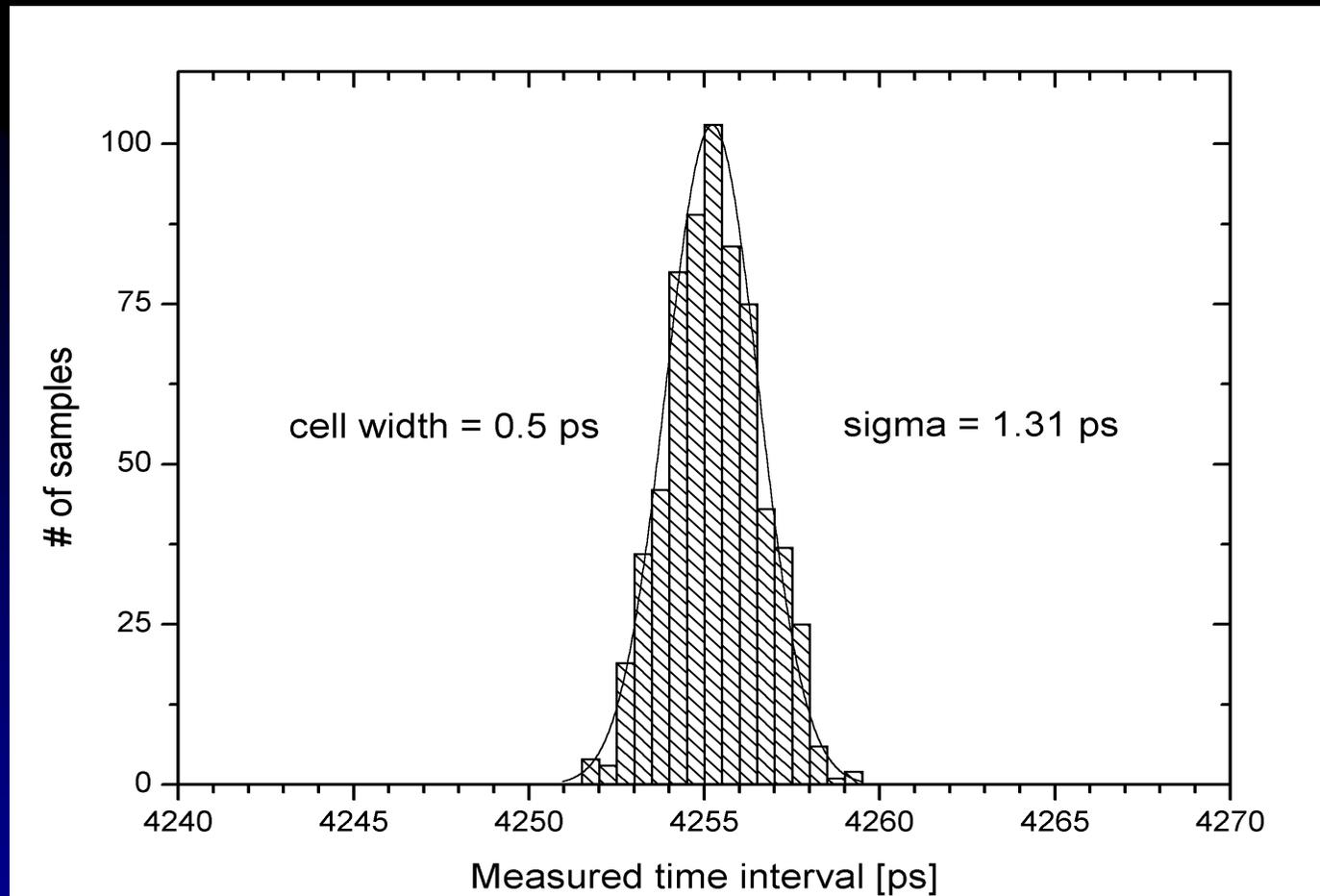
Two channels difference Tb-Ta
Jitter per channel ~ 920 fs

Timing tests set up
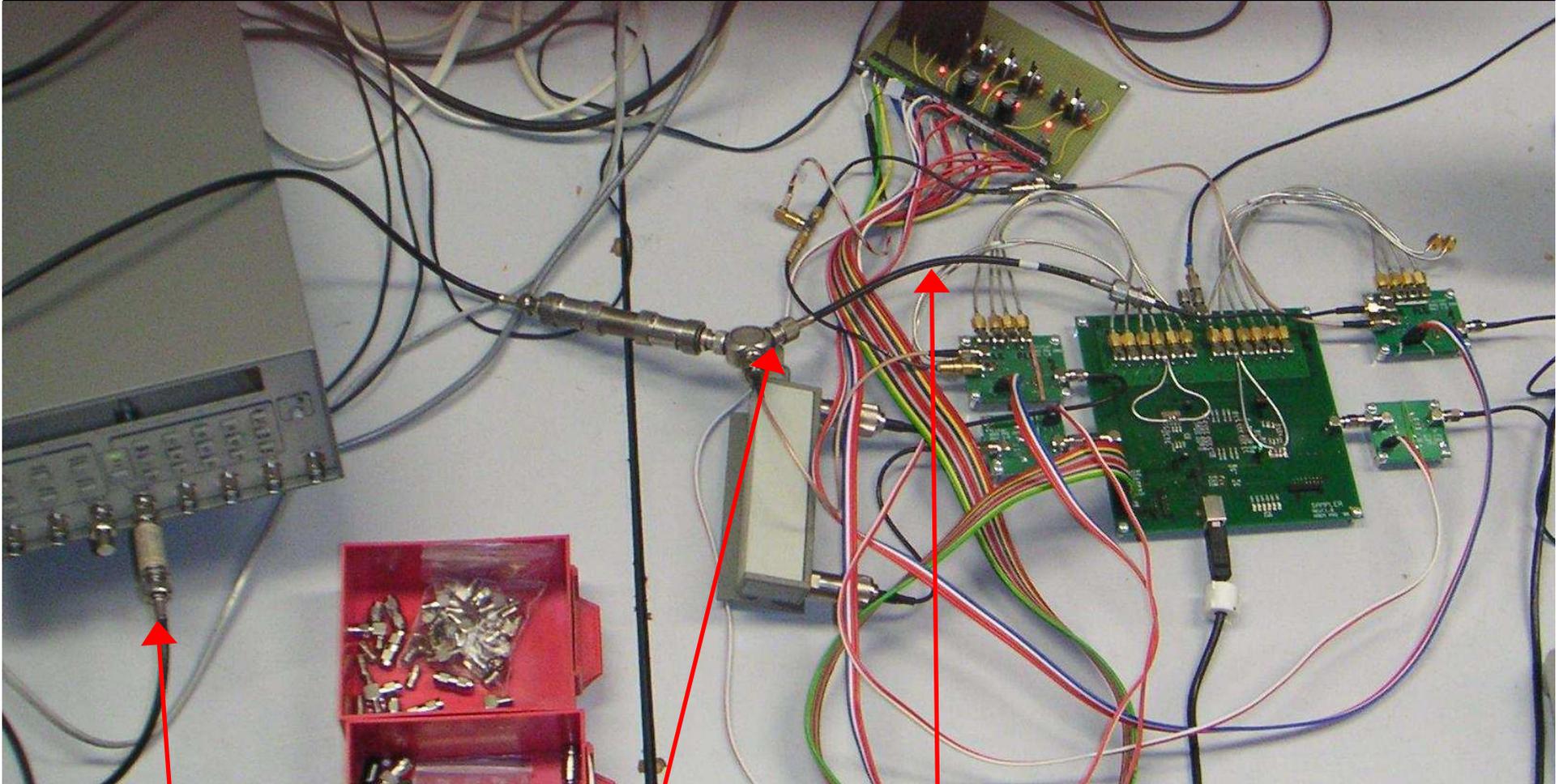
Pulse generator

Pulse divider   delay cable

Temperature drift - cable delay test

3 ps warm up

+/- 0.2 ps stabilityc

Prototype not tuned for temperature stability
Much lower values expected for final set up

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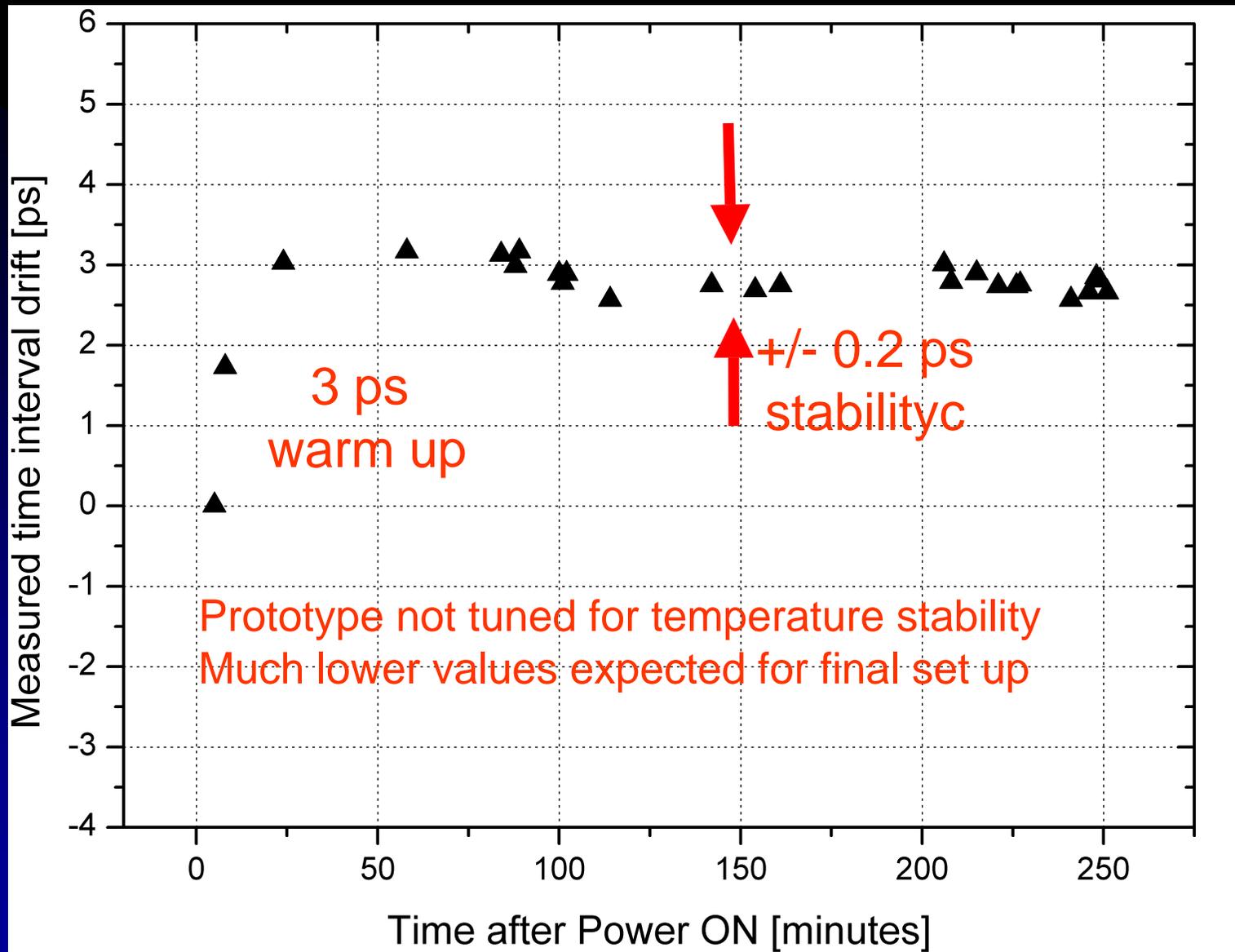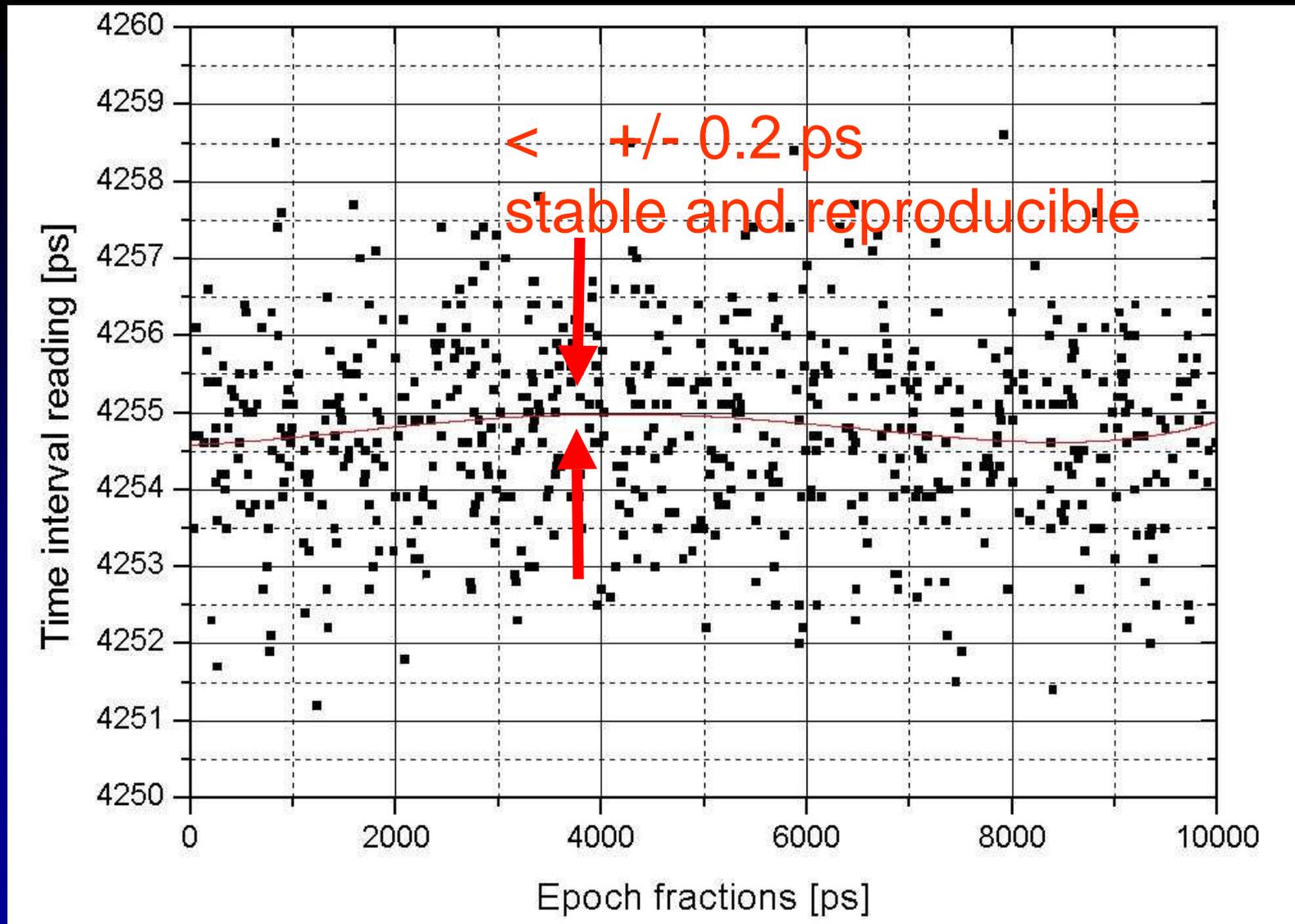
Timing linearity

Epoch timing device
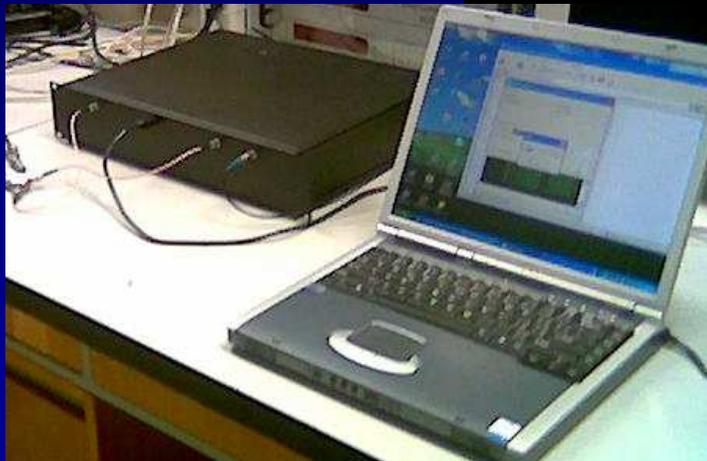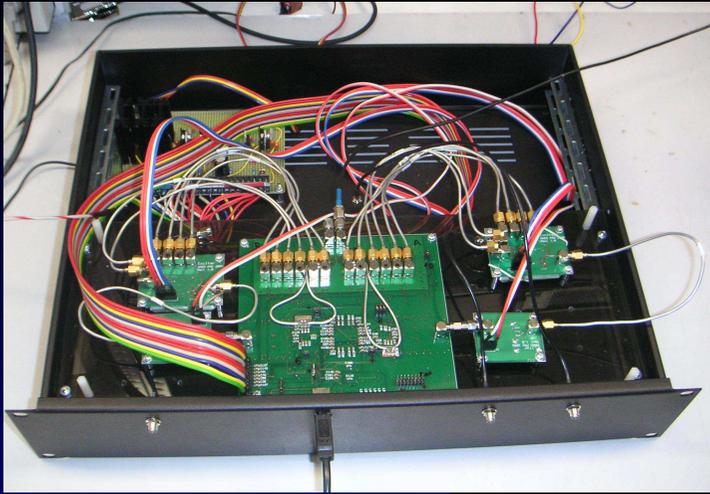
- Epoch timing system,
  Two independent channels

- Inputs   NIM

- Jitter   0.9 ps / ch
- Non-linearity   < 0.2 ps
- Stability   < +/- 0.2 ps
- Power   < 15 Watts
- Interface   USB
- Repetition rate   10 Hz max

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SLR tests in Graz, 4.3 km ground target

```
Data file GRAZ_FAR.TXT    coll. #   0
```

Graz ET
Dassault

8.0 ps jitter

```
500                 Cell width   3    Tic =    48.000000
   Criter.                    MEAN           SIGMA       PT #
500.000   /    740.000     638.419373     18.801394     868
   3 * SIGMA                638.552490      8.913544     829
   2.5*SIGMA                638.867859      7.965956     802
```

```
Data file far2.txt    coll. #   0
```

New PET
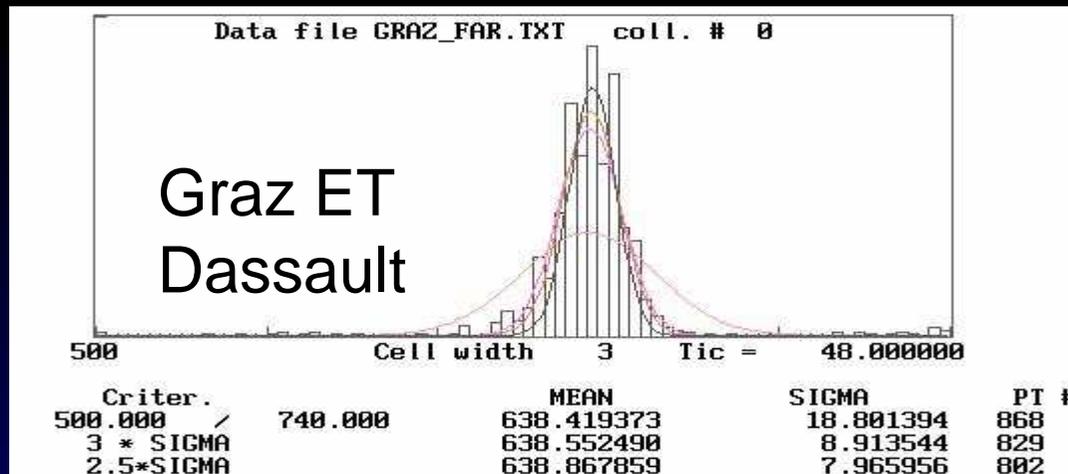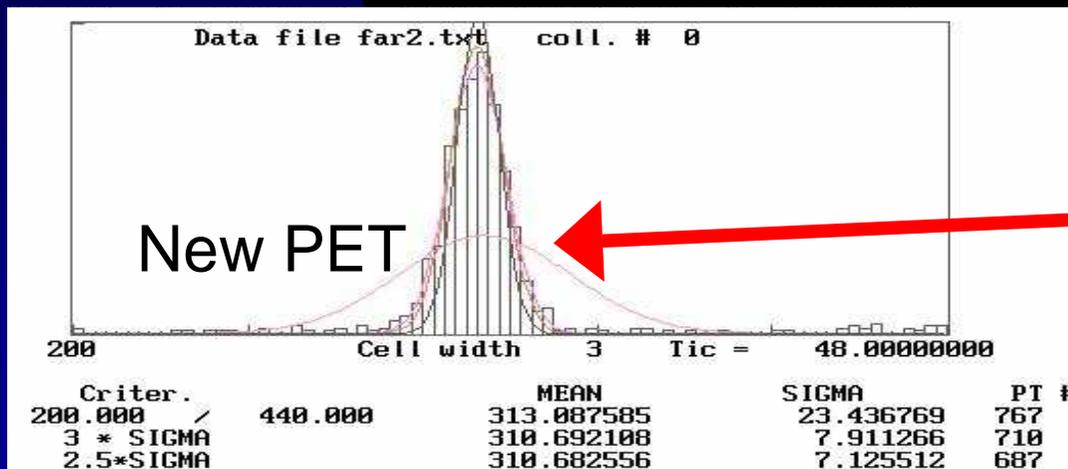
7.1 ps jitter

Normal distribution (!!)

```
200                 Cell width   3    Tic =    48.00000000
   Criter.                    MEAN           SIGMA       PT #
200.000   /    440.000     313.087585     23.436769     767
   3 * SIGMA                310.692108      7.911266     710
   2.5*SIGMA                310.682556      7.125512     687
```

The difference corresponds to 2.5 ps versus 0.9 ps
for Dassault and NPET timing jitters

Summary

- GOOD NEWS

- Sub – picosecond event timing device is existing

  - jitter < 1 ps / channel

  - non-linearity, stability < 0.2 ps

  - further improvement expected ☺

- The device is low power, compact, reliable

- The theoretical repetition rate limit is ~ 100 kHz ☺

- BAD NEWS

- The data processing is time consuming, maximum rep. rate is limited, 100 Hz expected soon

- new approaches are needed for kHz systems

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Conclusion

- Sub – picosecond event timing device is existing

- Novel timing principle (P.Panek) verified for the first time

- New technologies appreciated

- Self - calibrating device
  <u>no adjustment or calibration needed</u> ever

- Space version seems to be possible

- Looking for applications ☺

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